

Optimized Zero Vector Selection in Space Vector Pulse Density Modulation Schemes for Two-Level Inverter Fed Induction Motor Drive

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Abstract—Space Vector Pulse Density Modulation (SVPDM) schemes for adjustable speed drives are digital modulation scheme with less computational overhead. The SVPDM based drives provide better spectral features and reduced acoustic noise in motor than Space Vector Pulse Width Modulation (SVPWM) drives. The discontinuous nature of SVPDM scheme is investigated in this article to find optimized zero vector selection in SVPDM schemes for adjustable speed control of induction motor. Five types of Discontinuous SVPDM (DSVPDM) schemes for two-level inverter are proposed in this paper based on selection of zero vectors. Analysis is carried out to find the optimized zero vector selection. Performances of the proposed DSVPDM schemes are compared with existing SVPDM and popular space vector based Discontinuous Pulse Width Modulation schemes. The DSVPDM schemes are validated for a 11.5 kVA two-level inverter driving a 3-HP three-phase induction motor using dSpace DS1104 real time interface platform.

Index Terms—induction motor, inverter, sigma delta modulator, total harmonic distortion, vector quantization.

I. INTRODUCTION

To overcome the scarcity of fossil fuels and to mitigate the adverse effects of fossil fuels on environment, Electric Vehicles (EVs) are being promoted worldwide [1]. Extensive researches are being carried out recently in the field of practicality of EVs. Induction Motor (IM) for driving EVs are gaining popularity due to their high efficiency, low cost, ruggedness, reliability and less weight compared to DC motors for same nominal power [2]. IM is fed from a constant DC source through inverter in EV propulsion system. The adjustable speed control of IM is attained by changing the duty ratio of inverter switching signals. Space Vector Pulse Width Modulation (SVPWM) is preferred over Sine Triangle Pulse Width Modulation (SPWM) in Adjustable Speed Drives (ASD) of IM. SVPWM has better DC bus utilization and reduced harmonics compared to SPWM [3-4]. SVPWM provides full control over the switching sequences and it can be digitally implemented easily compared to SPWM [5].

The steps involved in SVPWM are identification of sector, calculation of duty ratio of switching vector of the sector and determination of optimum switching sequence [5-6]. In SVPWM, the power spectrum is concentrated at harmonics of switching frequency. This leads to acoustic

noise, electromagnetic interference and torque pulsation in IM [7].

Discontinuous Pulse Width Modulation (DPWM) techniques also known as Bus-Clamping PWM is proposed to reduce the switching loss in inverter [8-9]. In DPWM, the output of the inverter is clamped continuously to the DC bus over a period of time [8]. The acoustic noise components are reduced significantly in DPWM compared to SVPWM [10-11]. In SVPWM the zero vectors are placed in both sides of active vectors in a half cycle [5]. In DPWM schemes, only one of the zero vectors is selected so as to place the active vectors successively in two half cycles [8-11]. Advanced Bus-Clamping PWM schemes provide low harmonic distortion than DPWM by applying an active vector twice in a half cycle [12-13]. In Advanced Bus-Clamping PWM schemes one of the zero vector is not selected like DPWM. Generalized algorithm for space vector based DPWM schemes are proposed in [14-15].

The switching signals of an inverter can be considered as the output of an oversampling Analogue to Digital Converter (ADC) [16]. This resulted in applying oversampling ADC techniques in generating switching signals of inverter [16-22]. Sigma Delta Modulation (SDM), a digital modulation scheme, is a popular oversampling ADC technique. It is a pulse density modulation scheme with sample time equals to $1/f_s$, where f_s is the oversampling frequency [16]. Due to the noise shaping property of SDM, it spreads the power spectrum over a large bandwidth which suppresses acoustic noise in motor drive [16]. SVPDM provides better harmonic characteristics than SVPWM [16]. Due to their continuous spectrum it is difficult to identify the most significant harmonic voltage in Spread Spectral Schemes (SSS). Thus designing filters for SSS is challenging [23]. The minimum width of pulse in SVPDM schemes is the sampling time of SDM which ensures that the pulse width is always greater than ON time of switching devices [16]. SVPDM can be digitally implemented as they are digital modulation schemes [16].

In SVPDM scheme, the integrated error vector of SDM which follows the reference vector is quantized to its nearest space vector in a sample time to generate the switching vector. Thus it does not follow a specific switching sequence in which space vectors are selected in a sector [16]. This article investigates the discontinuous nature of SVPDM to find the optimized zero vector selection in a

sector for ASD of IM. The optimized zero vector selection in SVPDM is determined by analyzing the 3rd harmonic component of pole voltage. The 3rd harmonic component gives an account of Common Mode Voltage (CMV). CMV is responsible for the flow of bearing current in motor bearings which results in motor winding insulation breakdown and motor bearing damage [24]. In existing SVPDM [16] scheme for two-level inverter, zero vector V7 is selected for odd sectors and V0 is selected for even sectors. This results in increased 3rd harmonic content at lower modulation index which makes the existing SVPDM not suitable for ASD of IM. Five Discontinuous SVPDM (DSVPDM) schemes are proposed in this article. The DSVPDM schemes uses 3D triangular coordinate system as it inherits all the benefits of *mn* coordinate system and it simplifies the selection of nearest three switching vectors [25]. This article proposes that the 3rd harmonic component can be limited to around 20% for the entire modulation range in SVPDM by selecting same zero vectors for all sectors. The proposed schemes are simulated and validated using Matlab/Simulink software for a two-level inverter driving IM using open loop v/f control. The performance of proposed DSVPDM schemes are compared with existing SVPDM scheme and popular space vector based DPWM schemes. The DSVPDM schemes are implemented for a 11.5 kVA two-level inverter driving a 3-HP induction motor.

II. PROPOSED DISCONTINUOUS SVPDM SCHEMES

Fig. 1 shows the block diagram of proposed Discontinuous SVPDM schemes for two-level inverter.

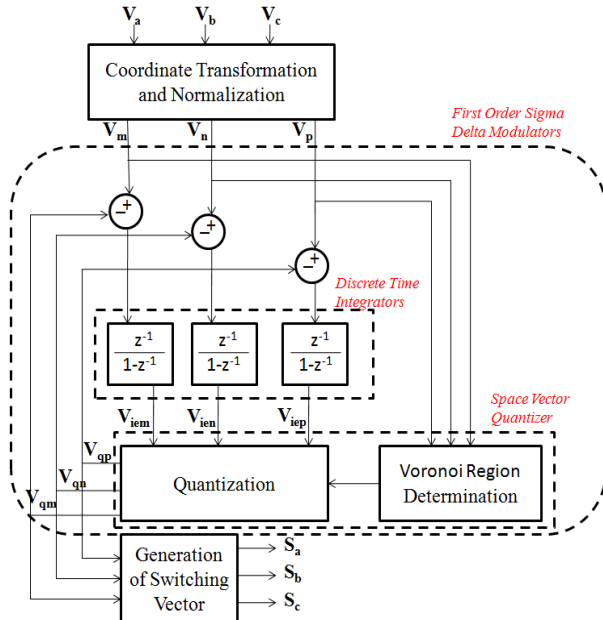


Figure 1. Block diagram of proposed scheme

The reference signal in *abc* coordinate system is transformed into the 3D triangular coordinate system (*mnp* coordinate system) and is normalized [25] to form normalized reference vector \mathbf{V}_{ref} (V_m, V_n, V_p). Proposed schemes use three first order sigma delta modulators with vector quantizer. The difference between normalized reference space vector (\mathbf{V}_{ref}) and quantized space vector \mathbf{V}_q (V_{qm}, V_{qn}, V_{qp}) are applied to discrete time integrators to

generate the integrated error vector \mathbf{V}_{ie} ($V_{iem}, V_{ien}, V_{iep}$). Integrated error vector \mathbf{V}_{ie} follows \mathbf{V}_{ref} . A space vector quantizer with step size one for *m*, *n* and *p* components is proposed. Depending on whether the normalized reference lies in odd sector or even sector the triangular voronoi region is determined and \mathbf{V}_{ie} is quantized to its closest space vector in voronoi region \mathbf{V}_q . The switching vector \mathbf{S}_w (S_a, S_b, S_c) in *abc* coordinate system are obtained from quantized space vector (\mathbf{V}_q). The simulink model of the proposed scheme is shown in Fig. 2. The proposed scheme is explained below in detail.

A. Generation of Normalized Reference Vector

In the 3D triangular coordinate system the axes *m*, *n* and *p* are mutually spaced at 60° apart. It corresponds to the line voltages a-b, b-c and c-a [25]. For a two-level inverter with dc bus voltage V_{DC} , the reference vector is normalized by dividing it with V_{DC} . The instantaneous normalized reference vector in 3D triangular coordinate system \mathbf{V}_{ref} (V_m, V_n, V_p) can be expressed as [25]

$$V_m = (V_a - V_b) \div V_{DC} \quad (1)$$

$$V_n = (V_b - V_c) \div V_{DC} \quad (2)$$

$$V_p = (V_c - V_a) \div V_{DC} \quad (3)$$

where, V_a , V_b and V_c are instantaneous phase voltages.

The switching states in 3D triangular coordinate system obtained by equations (1-3) for Two Level Inverter (TLI) are shown in Fig. 3. From Fig. 3 it is observed that the geometrical space encompassing the space vectors is a 3D hexagon with its fundamental sector being a triangle. All instantaneous values of \mathbf{V}_{ref} lie in the 3D hexagonal plane with equation $V_m + V_n + V_p = 0$.

B. Proposed Space Vector Quantizer

A space vector quantizer with step size one for *m*, *n* and *p* components is proposed in this paper. As the step size increases the difference between \mathbf{V}_{ref} and \mathbf{V}_{ie} increases [16]. The sector in which the reference vector lies forms the voronoi region. The difference between coordinates of \mathbf{V}_{ref} and vertices of sector in which it lies will be less than or equal to one, thus step size of the proposed quantizer is limited to one. \mathbf{V}_{ie} is quantized to its nearest space vector in the sector. Let $\mathbf{X}(X_m, X_n, X_p)$, $\mathbf{Y}(Y_m, Y_n, Y_p)$ and $\mathbf{Z}(Z_m, Z_n, Z_p)$ be the vertices of the sector in which \mathbf{V}_{ref} lies.

In order to obtain the vertices of the sector in which \mathbf{V}_{ref} lies, an intermediate space vector $\mathbf{I}(I_m, I_n, I_p)$ is determined.

$$I_m = \text{floor}(V_m) \quad (4)$$

$$I_n = \text{floor}(V_n) \quad (5)$$

$$I_p = -(I_m + I_n) \quad (6)$$

where, $\text{floor}()$ rounds the value to its nearest lowest integer.

If I_p satisfies condition (7) then \mathbf{V}_{ref} lies in an odd sector as shown in Fig. 4(a) and if I_p does not satisfies condition (7) then \mathbf{V}_{ref} lies in an even sector as shown in Fig. 4(b).

$$\text{abs}(V_p - I_p) \leq 1 \quad (7)$$

The nearest three space vectors of \mathbf{V}_{ref} can be expressed in terms of $\mathbf{I}(I_m, I_n, I_p)$ as

$$\mathbf{X} = \begin{cases} \begin{bmatrix} I_m \\ I_n \\ I_p \end{bmatrix}^T, & \text{if sector is odd} \\ \begin{bmatrix} I_m + 1 \\ I_n + 1 \\ I_p - 2 \end{bmatrix}^T, & \text{if sector is even} \end{cases} \quad (8)$$

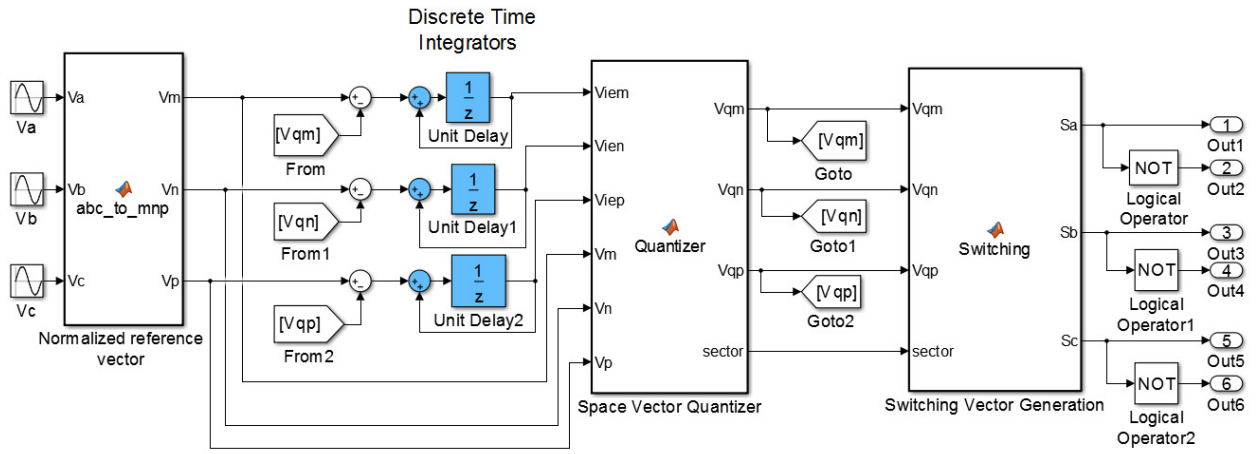


Figure 2. Simulink model of proposed scheme

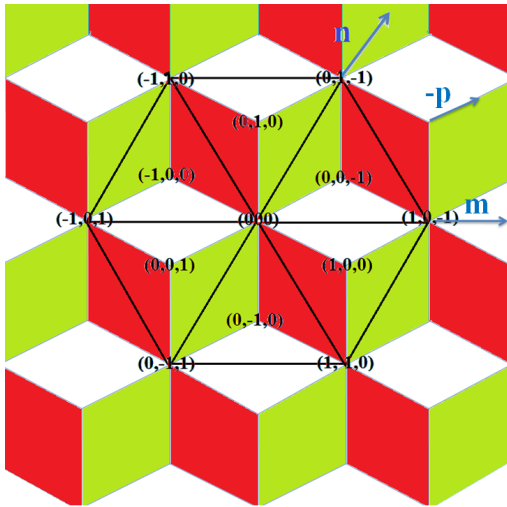


Figure 3. Normalized space vector diagram of two-level inverter in 3D triangular coordinate system

$$Y = [I_m + 1, I_n, I_p - 1]^T \quad (9)$$

$$Z = [I_m, I_n + 1, I_p - 1]^T \quad (10)$$

In order to illustrate how the vertices of sector in which V_{ref} lies is determined from instantaneous value of V_{ref} two examples are considered. If angle of phase-a voltage is θ , then the angle made by the resultant space vector with respect to a-axis ωt is $90^\circ - \theta^\circ$ (Fig. 5).

In the first example the instantaneous phase voltages at $\theta = 110^\circ$ for modulation index 0.8 are taken (sector 6). Here $V_m = 0.9074$, $V_n = -0.3151$ and $V_p = -0.5923$. Using the equations (4) to (6),

$I_m = \text{floor}(0.9074) = 0$, $I_n = \text{floor}(-0.3151) = -1$, $I_p = -(0 + -1) = 1$. The intermediate space vector I is $(0, -1, 1)$.

Here $\text{abs}(V_p - I_p) = \text{abs}(-0.5923 - 1) = 1.5923 > 1$. I_p does not satisfy condition (7) therefore V_{ref} lies in an even sector. By equations (8) to (10), the vertices of sector X , Y and Z are $(1, 0, -1)$, $(1, -1, 0)$ and $(0, 0, 0)$ which are the vertices of sector 6 (Fig. 3).

In the second example the instantaneous phase voltages at $\theta = 35^\circ$ for modulation index 0.8 are taken (sector 1). Here $V_m = 0.0803$, $V_n = -0.7548$ and $V_p = -0.8351$. Using the equations (4) to (6),

$I_m = \text{floor}(0.0803) = 0$, $I_n = \text{floor}(0.7548) = 0$, $I_p = -(0 + 0) = 0$. The intermediate space vector I is $(0, 0, 0)$.

Here $\text{abs}(V_p - I_p) = \text{abs}(-0.8351 - 0) = 0.8351 < 1$. I_p satisfy condition (7) therefore V_{ref} lies in an odd sector. By equations (8) to (10), the vertices of sector X , Y and Z are $(0, 0, 0)$, $(1, 0, -1)$ and $(0, 1, -1)$ which are the vertices of sector 1 (Fig. 3).

Euclidean distance between V_{ie} and vertices of voronoi region $X(X_m, X_n, X_p)$, $Y(Y_m, Y_n, Y_p)$ and $Z(Z_m, Z_n, Z_p)$ are determined. The space vector having minimum euclidean distance with V_{ie} is selected as the quantized space vector $V_q(V_{qm}, V_{qn}, V_{qp})$.

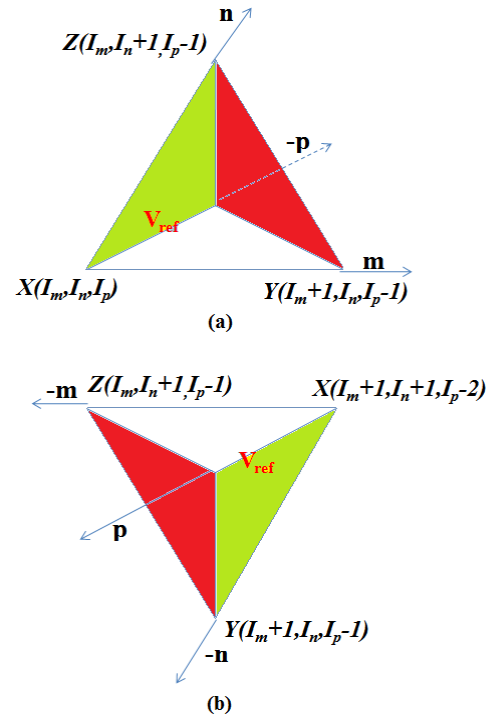


Figure 4. Voronoi region

C. Generation of Switching Vector

The switching vector in abc coordinate system (S_a, S_b, S_c) are obtained from the quantized space vector $V_q(V_{qm}, V_{qn}, V_{qp})$. Comparing the space vectors in abc coordinate system (Fig. 5) with corresponding space vectors in 3D triangular coordinate system (Fig. 3) the following relation is obtained for generating the active space vectors.

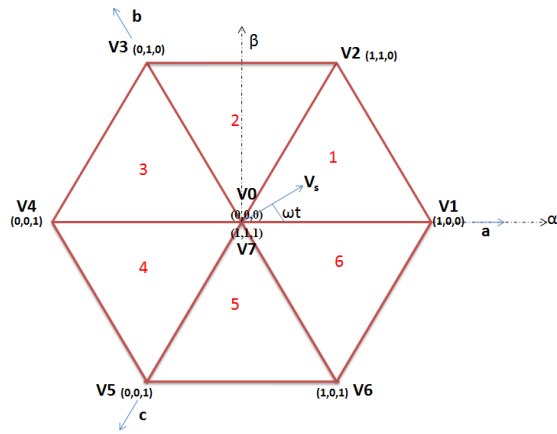


Figure 5. Space vector diagram of two-level inverter in abc coordinate system

$$[S_a, S_b, S_c]^T = \begin{cases} [1, 0, V_{qm} + V_{qp}]^T, & \text{if } \text{sign}(V_{qm}) \text{ is } 1 \\ [V_{qm} + V_{qn}, 1, 0]^T, & \text{if } \text{sign}(V_{qn}) \text{ is } 1 \\ [0, V_{qn} + V_{qp}, 1]^T, & \text{if } \text{sign}(V_{qp}) \text{ is } 1 \end{cases} \quad (11)$$

where, $\text{sign}()$ gives output as 1, 0 and -1 if the value is positive, zero and negative respectively.

If neither of V_{qm} , V_{qn} or V_{qp} is positive then quantized space vector V_q is a zero vector. The selection of zero vectors in different sectors will result in different discontinuous modulation schemes.

D. Proposed Discontinuous Modulation Strategies

Five discontinuous modulation schemes for SVPDM are defined in this paper. The first scheme termed as DSVPDMmin takes zero vector V_0 (000) for all sectors. The zero vector placements in all sectors for DSVPDMmin are shown in Fig. 6(a). In the second scheme DSVPDMmax zero vector V_7 (111) is selected for all sectors (Fig. 6(b)). In the third scheme termed as DSVPDM0 zero vector V_0 (000) is selected for all even sectors and zero vector V_7 (111) is selected for all odd sectors (Fig. 6(c)). In the fourth proposed scheme DSVPDM1 both zero vectors V_0 (000) and V_7 (111) are selected for each sector. In the odd sectors for the first 30° zero vector V_7 is selected and for the next 30° zero vector V_0 is selected. In the even sectors for the first 30° zero vector V_0 is selected and for next 30° zero vector V_7 is selected. The zero vector placements in DSVPDM1 is shown in Fig. 6(d). The criteria used to determine zero vectors in DSVPDM1 is given in (12) [16]. In the fifth scheme DSVPDM2 zero vector V_0 (000) is selected for all odd sectors and zero vector V_7 (111) is selected for all even sectors (Fig. 6(e)).

The switching vectors selected for proposed SVPDM schemes in different sectors are shown in Table I. Fig. 7 shows the clamping of a-phase pole voltage for the proposed schemes with respect to different sectors of space vector diagram. For all the five proposed discontinuous SVPDM schemes the pole voltage is clamped for a period of 120° .

$$\begin{cases} V_7 \text{ is selected, if } ((V_a \times V_b \times V_c)^3) > 0 \\ V_0 \text{ is selected, otherwise} \end{cases} \quad (12)$$

where, V_a , V_b and V_c are instantaneous phase voltages.

The SVPDM scheme [16] uses $\alpha\beta$ coordinates, hence the integrated error vector needs to be converted to abc coordinates to generate the switching vector.

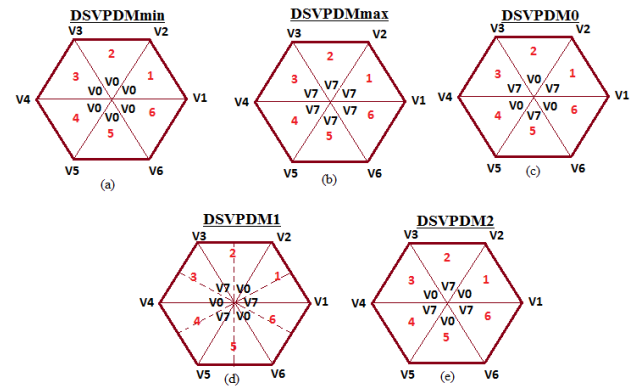


Figure 6. Zero Vector placement in proposed DSVPDM schemes for sectors 1-6: (a) DSVPDMmin; (b) DSVPDMmax; (c) DSVPDM0; (d) DSVPDM1; (e) DSVPDM2



Figure 7. Clamping of a-leg pole voltage for the proposed schemes in sector 1-6 for the five Discontinuous SVPDM schemes

TABLE I. SWITCHING VECTORS SELECTED IN PROPOSED DSVPDM SCHEMES IN DIFFERENT SECTORS

Proposed Schemes	Sector					
	1	2	3	4	5	6
DSVPDMmin	V1	V2	V3	V4	V5	V6
	V2	V3	V4	V5	V6	V1
	V0	V0	V0	V0	V0	V0
DSVPDMmax	V1	V2	V3	V4	V5	V6
	V2	V3	V4	V5	V6	V1
	V7	V7	V7	V7	V7	V7
DSVPDM0	V1	V2	V3	V4	V5	V6
	V2	V3	V4	V5	V6	V1
	V7	V0	V7	V0	V7	V0
DSVPDM1	V1	V2	V3	V4	V5	V6
	V2	V3	V4	V5	V6	V1
	V0	V0	V0	V0	V0	V0
DSVPDM2	V1	V2	V3	V4	V5	V6
	V2	V3	V4	V5	V6	V1
	V0	V7	V0	V7	V0	V7

The switching vectors are again converted to $\alpha\beta$ coordinates to provide the feedback for Sigma Delta Modulator. In the proposed DSVPDM schemes the switching vector in abc coordinates are obtained from the quantized space vector in 3D triangular coordinate system directly. Thus the feedback signals for SDM need not be generated separately in the proposed schemes. In SVPDM scheme [16] the space vector diagram is divided into seven non overlapping voronoi regions and a particular code vector is assigned to a voronoi region. In the proposed DSVPDM schemes the integrated error vector is quantized to nearest space vector of the sector in which reference vector lies, to minimize the deviation of integrated error vector from reference vector.

E. Optimized Zero Vector Selection in SVPDM Scheme

In DSVPDM schemes the integrated error vector is quantized to its nearest space vector. At lower modulation index the instances at which the integrated error vector getting quantized to zero vectors is more. Thus the optimum

zero vector selection in DSVPDM may not be same as in DPWM. In order to analyze the effect of zero vector selection in DSVPDM schemes the 3rd harmonic content of pole voltage is considered. In Fig. 8 the 3rd harmonic content of pole voltage obtained for proposed DSVPDM schemes, SVPDM and SVPWM are plotted. In DSVPDMmin and DSVPDMmax where zero vector **V0** and **V7** are selected respectively for all sectors, the 3rd harmonic component retains its value around 20% similar to SVPWM. In DSVPDM1 at high modulation indexes the 3rd harmonic component is lower than 20%. At modulation index 0.8 and 0.7 the 3rd harmonic component obtained for DSVPDM1 is 4.56% and 12.53% respectively. As modulation index decreases the 3rd harmonic component of DSVPDM1 increases and it reaches over 150% at modulation index 0.3. In SVPDM, DSVPDM2 and DSVPDM0 the 3rd harmonic component of pole voltage is around 20% at modulation index 0.8. It increases as modulation index is decreased and reaches over 160% at modulation index 0.3. From Fig. 8 it can be inferred that DSVPDMmin and DSVPDMmax are the suitable schemes for adjustable speed drive of induction motor. DSVPDM1 can be used in high speed applications as it gives lower 3rd harmonic component at high modulation indexes. DSVPDM1 and DSVPDMmin can be combined for ASD such that for modulation index greater than or equal to 0.7 zero vectors are selected as in DSVPDM1 and **V0** is selected otherwise.

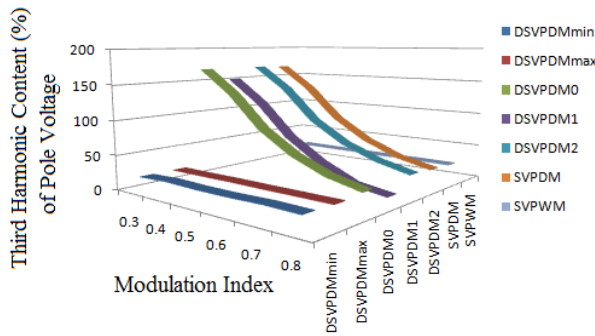


Figure 8. Comparison of 3rd harmonic component of pole voltage obtained for proposed DSVPDM schemes, SVPDM and SVPWM

The switching vector **V0** (000) and **V7** (111) results is zero phase voltage. In the proposed DSVPDM schemes since the active vectors selected are same, the phase voltage will also remain same. Thus zero vector placements do not have any effect on phase voltage and motor phase current. Total Harmonic Distortion (THD) of phase voltage and motor phase current of proposed DSVPDM schemes are shown in Fig. 9 and Fig. 10 respectively. It can be observed that THD does not vary for phase voltage and motor phase current for proposed DSVPDM schemes. Pole voltage is the sum of phase voltage and Common Mode Voltage (CMV). The waveforms extracted by lowpass filtering pole voltage, phase voltage and CMV of the proposed schemes are shown in Fig. 11. Since the five DSVPDM schemes have similar phase voltage their common mode voltage varies depending on zero vector selection.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed DSVPDM schemes are implemented for a

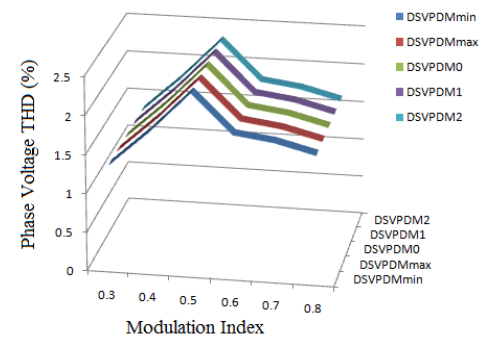


Figure 9. THD% of phase voltage obtained for proposed DSVPDM schemes

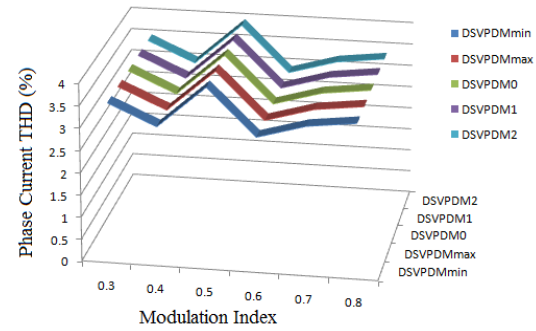


Figure 10. THD% of motor phase current obtained for proposed DSVPDM schemes

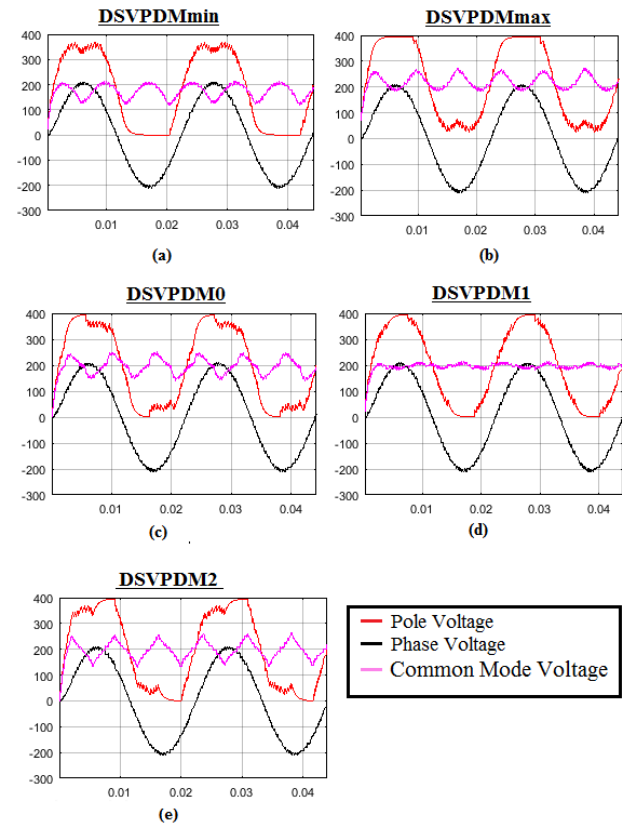


Figure 11. Waveforms extracted by low pass filtering Pole Voltage, Phase Voltage and Common Mode Voltage of the proposed schemes

11.5 kVA two-level inverter driving a 3-HP induction motor using open loop v/f control. The experimental setup is shown in Fig. 12. dSpace DS1104 RTI platform is used to implement the proposed schemes with a sampling frequency of 20 kHz. The a-phase pole voltage, phase voltage and motor phase current obtained for proposed schemes and SVPDM at modulation index 0.8 is shown in Fig. 13.

In Fig. 13 the first trace shows pole voltage, second trace

shows phase voltage and third trace shows the motor current. The zero vector selection in proposed DSVPDMmin, DSVPDMmax, DSVPDM0, DSVPDM1 and DSVPDM2 is similar to DPWMmin, DPWMmax, DPWM0, DPWM1 and DPWM2 respectively [15]. In DSVPDMmin the pole voltage is clamped to 0 V from 210° to 330° (Fig. 13(a)). In DSVPDMmax the pole voltage is clamped to 100 V from 30° to 150° (Fig. 13(b)). In DSVPDM0 the pole voltage is clamped to 100 V from 30° to 90° and clamped to 0 V from 210° to 270° (Fig. 13(c)). In DSVPDM1 the pole voltage is clamped to 100 V from 60° to 120° and clamped to 0 V from 240° to 300° (Fig. 13(d)). In DSVPDM2 the pole voltage is clamped to 100 V from 90° to 150° and clamped to 0 V from 270° to 330° (Fig. 13(e)). The phase voltage and motor current are same for the proposed schemes (Fig. 13).

The 3rd harmonic component of pole voltage obtained experimentally for proposed schemes, SVPDM and SVPWM at modulation index 0.8 and 0.4 are shown in Table II.

The 3rd harmonic components are obtained using the FFT analysis feature of digital oscilloscope. DSVPDMmin and DSVPDMmax have 3rd harmonic component around 20% similar to SVPWM at both modulation index 0.8 and 0.4 (Table II). This shows that the optimum zero vector placement in SVPDM schemes for adjustable speed drive of induction motor is either selecting **V0** for all sectors (DSVPDMmin) or **V7** for all sectors (DSVPDMmax).

At modulation index 0.8 the 3rd harmonic component of pole voltage of DSVPDM1 is 80.28% lower than SVPWM,

79.6% lower than DSVPDMmin and 79.1% lower than DSVPDMmax (Table II). This makes DSVPDM1 a better modulation technique for high speed applications.

TABLE II. THIRD HARMONIC COMPONENT OF POLE VOLTAGE

Schemes	3 rd Harmonic component of Pole Voltage	
	Modulation index 0.8	Modulation index 0.4
DSVPDMmin	20.5%	20.6%
DSVPDMmax	20%	19.9%
DSVPDM0	23.9%	134%
DSVPDM1	4.18%	116%
DSVPDM2	22.7%	132%
SVPDM	22.3%	131%
SVPWM	21.2%	21.1%

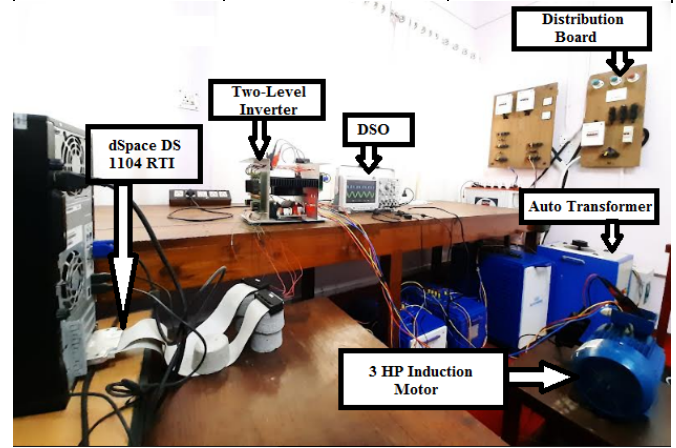


Figure 12. Experimental setup

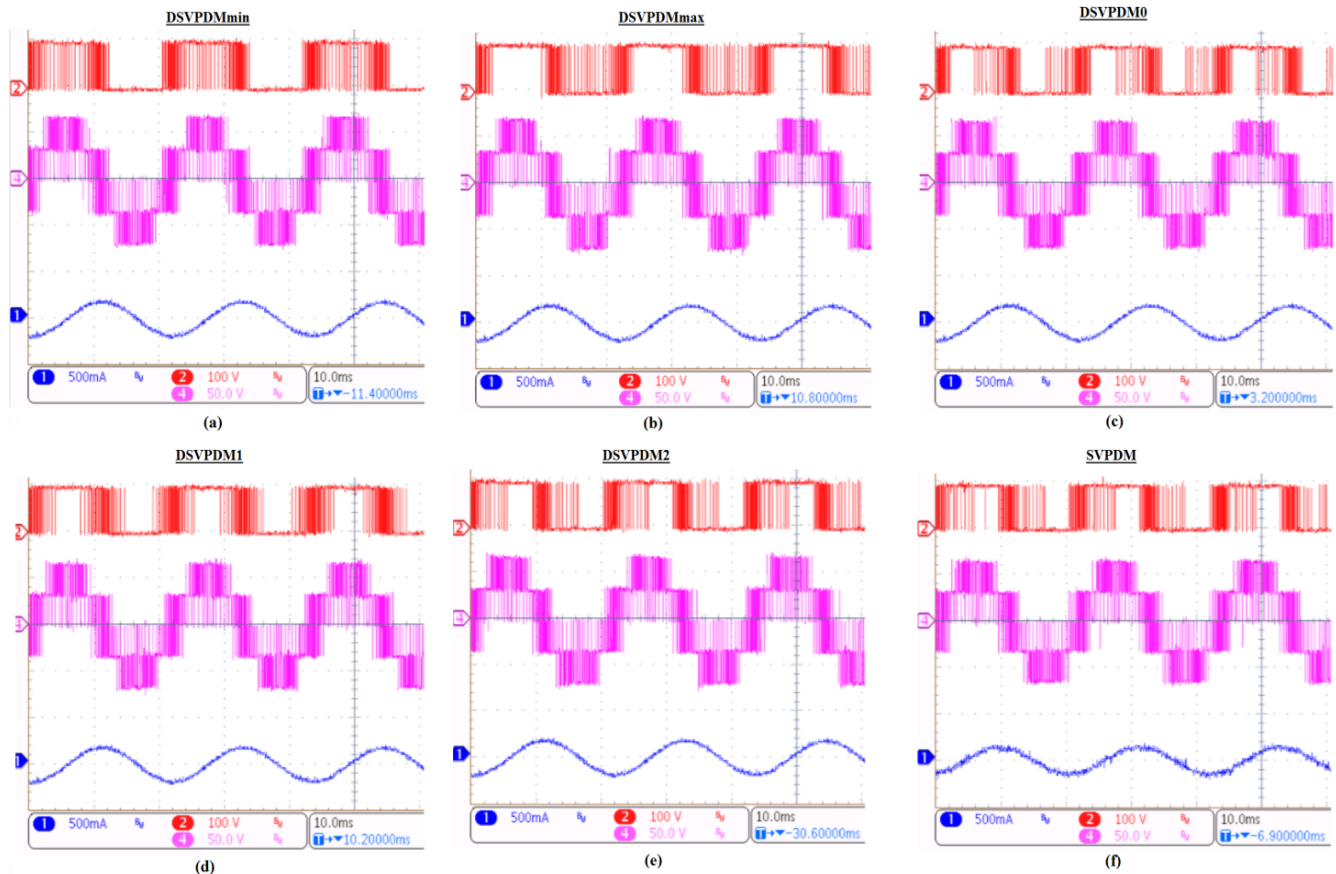


Figure 13. Pole Voltage (V_{AO}), Phase Voltage (V_{AN}) and Phase Current (I_A) at modulation index 0.8 for: (a) DSVPDMmin, (b) DSVPDMmax, (c) DSVPDM0, (d) DSVPDM1, (e) DSVPDM2 and (f) SVPDM. Scale: For upper trace (V_{AO}), Y-axis: 100V/div, middle trace (V_{AN}), Y-axis: 50 V/div and lower trace (I_A), Y-axis: 500 mA/div. X-axis: 10ms/div

IV. COMPARISON WITH EXISTING SCHEMES

The number of switching per cycle of reference signal obtained for proposed DSVPM schemes, SVPDM and DPWM schemes is shown in Fig. 14. The proposed DSVPM schemes has less switching per cycle than DPWM schemes.

THD of phase voltage and motor phase current obtained for proposed DSVPM schemes is compared with SVPDM and DPWM schemes in Fig. 15 and Fig. 16 respectively. The proposed DSVPM schemes shows better THD characteristics than SVPDM, DPWM0, DPWM1, DPWM2 and DPWM3 over the entire modulation range. At higher modulation index the proposed DSVPM schemes have better THD characteristics than DPWMmin and DPWMmax.

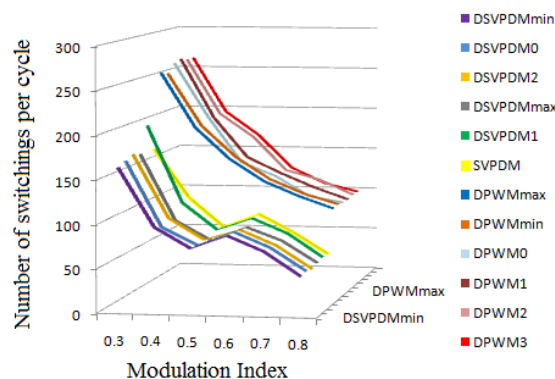


Figure 14. Comparison of Number of switching per cycle obtained for proposed DSVPM schemes with SVPDM and DPWM schemes

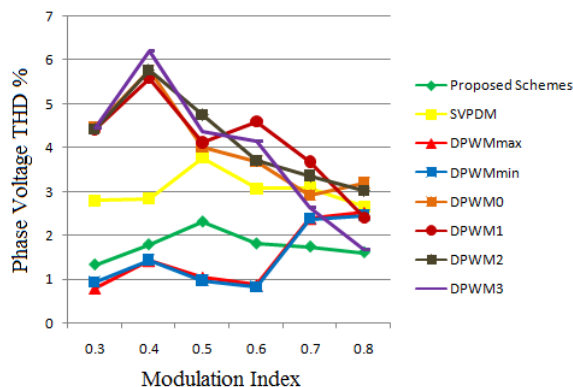


Figure 15. Comparison of THD% of phase voltage obtained for proposed DSVPM schemes with SVPDM and DPWM schemes

To analyze the DC bus utilization of DSVPM schemes the fundamental voltage obtained for proposed DSVPM schemes, SVPDM and DPWM schemes are plotted in Fig. 17. From Fig. 17 it can be observed that the fundamental voltage of proposed DSVPM schemes, SVPDM and DPWM schemes are same. This shows that DSVPM schemes have DC bus utilization similar to DPWM schemes and SVPDM.

V. CONCLUSION

For Space Vector Pulse Density Modulation (SVPDM) schemes the inverter output is clamped for 120° in a cycle irrespective of how zero vectors are selected and it is a discontinuous modulation scheme. Selecting same zero

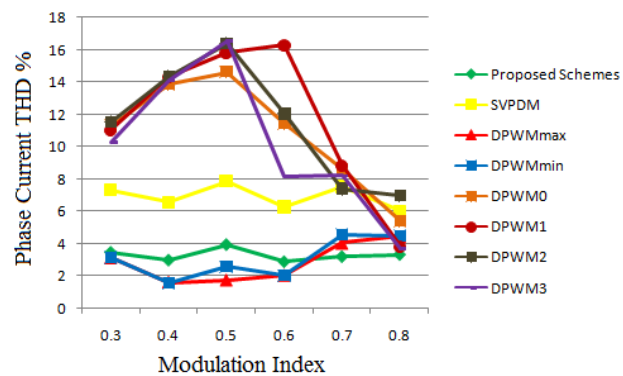


Figure 16. Comparison of THD% of motor phase current obtained for proposed DSVPM schemes with SVPDM and DPWM schemes

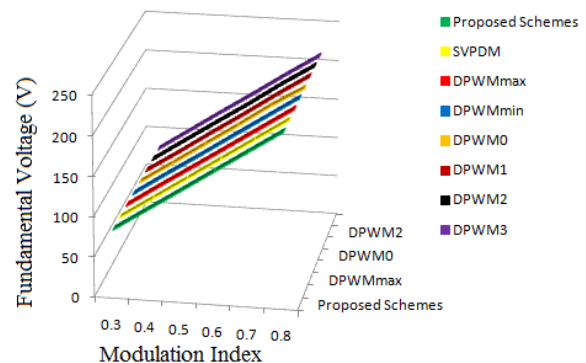


Figure 17. Comparison of fundamental voltage obtained for proposed DSVPM schemes with SVPDM and DPWM schemes

vectors for all sectors gives optimized SVPDM scheme for adjustable speed control of Induction Motor (DSVPMmin, DSVPMmax).

This results in retaining the 3rd harmonic component of pole voltage to around 20% for all modulation indexes. Selecting zero vectors such as to clamp the pole voltage to positive DC bus during 60° to 120° and negative DC bus during 240° to 300° (DSVPM1) will give reduced 3rd harmonic content at higher modulation index. The proposed schemes are validated experimentally. In DSVPM schemes the way in which zero vectors are selected does not affect the phase voltage and phase current. The performance of proposed DSVPM schemes are compared with existing SVPDM scheme and popular space vector based DPWM schemes. The proposed DSVPM schemes show better THD characteristics for phase voltage and phase current. The proposed DSVPM schemes have DC bus utilization similar to SVPDM and space vector based DPWM schemes.

ACKNOWLEDGMENT

J.M.P thanks Kerala State Council for Science Technology and Environment for their support in the form of Research Fellowship.

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