

A Power Electronic Traction Transformer Model for a New Medium Voltage DC Electric Railway

Izsák FERENCZ, Dorin PETREUȘ

Department of Applied Electronics, Technical University of Cluj-Napoca, 400027, Romania
 izsak.ferencz@ael.utcluj.ro

Abstract—All state-of-the-art Power Electronic Traction transformers (PETT) were developed for the existent Medium Voltage (MV) AC Electric Railway Systems (ERS). This work, however, presents a PETT for a novel MVDC-ERS. We studied and evaluated various state-of-the-art PETT topologies in two previous articles to determine which is best for this application, and we presented an 8-module Input Series Output Parallel (ISOP) MVDC PETT with a total power exceeding 1.2 MW. The converter topology used in the modules is the Dual Active Bridge (DAB). In this paper, the complete mathematical model of the converter, the deduction of controller parameters and the decoupling method, and the simulation model are presented in detail. Simulations show how the system works and interacts with a traction motor, as well as its response to input voltage variation and load steps. The results and theoretical notions obtained in this project will lay the foundation of a novel smart MVDC-ERS, meanwhile an experimental prototype is under development.

Index Terms—DC-DC power converters, traction power supplies, railway engineering, modular construction, Silicon carbide.

I. INTRODUCTION

This is an extended version of the paper [1], which presented a power electronic traction transformer for MVDC electrification. PETTs are the new trend in electric railway traction, because of higher efficiency and power density. Such systems achieve these using Medium Frequency Transformers (MFT) in the converter modules as galvanic separation. State of the art PETTs use Wide Band Gap (WBG) semiconductors to increase total efficiency. In the past, lacking mature semiconductor and material technology, MVDC railway electrification was not possible to be implemented, therefore MVAC railway electrification became the most popular and in some areas low voltage DC systems [2]. In our previous article [3], the MVDC and MVAC railway electrification systems were already compared in detail. The new system combines the advantage of a DC system with the advantages of using medium-voltage [4-9]. Moreover, in [3], after an overview of state of the art topologies [10], the modular ISOP structure is chosen with a DAB and a bidirectional phase-shift converter – both now implemented in Simulink.

Modular energy conversion systems are popular in many power applications like renewables and electric vehicles [11-12]. In this paper, the detailed mathematical model of the DAB converter, its connection in ISOP and the compensator design is deduced. Then the Matlab/Simulink

model and simulations of a whole MVDC catenary-line fed traction system is presented. Since in [13], N. Mohan demonstrates that in an ISOP system, the same control loop applied for all modules will achieve stability, therefore the first step in the project was to implement the system with a single control loop. After successful simulation however, based on [14] the system was further developed. In [14] it is stated, that due to input voltage or inductance mismatch in modules, one control loop for all modules may not reach a well-balanced input stage and the article presents a decoupling method for a 3 modules system in ISOP connection. In our paper, starting from a model with four modules, the generic form and formulas for systems with N modules are derived [1] and then successfully applied on our PETT system with eight modules. A traction drive and motor is also attached to the transformer to demonstrate its capability to power a traction motor.

Figure 1 below illustrates the concept of PETTs in a MVDC system (third) compared to conventional low voltage DC (first) and MVAC (second) railway systems. In the figure, M stands for Motor and it is attached through an inverter to the output.

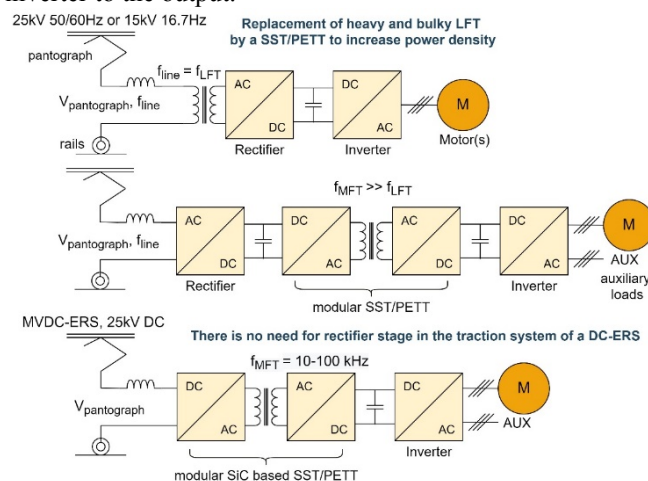


Figure 1. PETT in MVDC-ERS systems compared to traditional ERS

The modular DC-DC PETT stage uses Silicon Carbide (SiC) semiconductor devices to achieve higher power density. The paper also includes a short sum up about their advantages compared to other WBG devices.

The paper is structured as follows: section 2 presents the detailed mathematical model of the DAB converter with its average and small signal model, then section 3 contains the mathematical model of the converter in ISOP connection and the deductions of the decoupling control strategy for N modules. In section 4 the simulation model and results are discussed together with some considerations on WBG semiconductors. Finally, section 5 draws the conclusions.

This project has received funding from the Shift2Rail Joint Undertaking (JU) under grant agreement No 826238. The JU receives support from the European Union's Horizon 2020 research and innovation programme and the Shift2Rail JU members other than the Union.

II. DAB CONVERTER – MATHEMATICAL MODEL

The mathematical model of a phase-shift (between primary and secondary bridge) controlled DAB converter can be derived starting from the detailed analysis of the current and voltage waveforms of the leakage inductor. Based on the obtained equations the average model will be deduced [15]. As seen on Fig. 2a), for the interval $0 < t < d \cdot T$, the voltage on the leakage inductor is the sum of the input voltage – denoted by v_i , and the output voltage reflected in the primary – denoted by v_o' (v_o' is v_o over n , where n is the transformer turn ratio). Similarly, for the interval $d \cdot T < t < T$ the inductor voltage is $v_i - v_o'$ and d is the phase-shift between the two bridges. Therefore, the inductor voltage has the following equation as a function of the value of the inductor – L_{lk} , the half of the switching period – T , and the peak values of the inductor current – I_1 and I_2 .

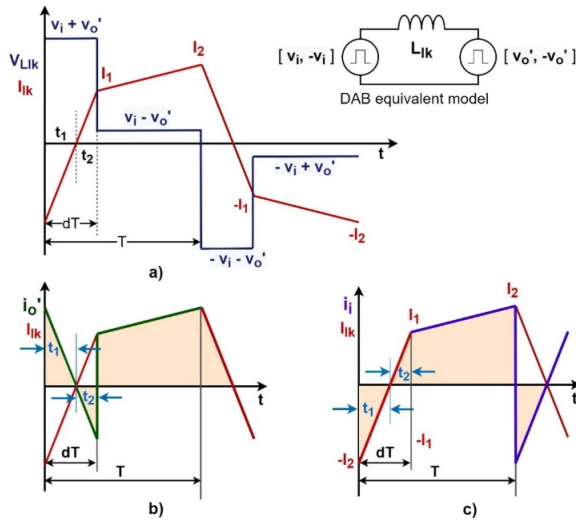


Figure 2. DAB converter - waveforms: a) presents the leakage inductor voltage and current, b) shows the output current reflected in the primary, compared to the leakage inductor current i_L and c) represents the input current compared to i_L .

$$V_{Llk} = \begin{cases} v_i + v_o' = L_{lk} \frac{I_1 + I_2}{d \cdot T}, & \text{for } 0 < t < dT \\ v_i - v_o' = L_{lk} \frac{I_2 - I_1}{(1-d) \cdot T}, & \text{for } dT < t < T \end{cases} \quad (1)$$

To obtain the value of the two peaks of the current, I_2 and I_1 , the two equations from (1) have to be added and then subtracted:

$$I_1 = \frac{T}{2L_{lk}} (2dv_i + v_o' - v_i) \quad (2)$$

$$I_2 = \frac{T}{2L_{lk}} (2dv_o' + v_i - v_o') \quad (3)$$

Looking at Fig. 2.b) and 2.c), $d \cdot T$ has two subintervals, of length t_1 and t_2 with the following conditions:

$$t_1 + t_2 = d \cdot T \quad (4)$$

$$I_2 \cdot t_2 = I_1 \cdot t_1$$

From (3) t_1 and t_2 is obtained:

$$t_1 = T \frac{2dv_o' + v_i - v_o'}{2(v_o' + v_i)} \quad (5)$$

$$t_2 = T \frac{2dv_i + v_o' - v_i}{2(v_o' + v_i)} \quad (6)$$

Using the peak values I_1 and I_2 and the time intervals t_1 and t_2 , the average input and output current can be calculated, using Fig. 2.b) and 2.c):

$$i_{i,avg} = \frac{1}{T} \left[-\frac{1}{2} I_2 t_1 + \frac{1}{2} I_1 t_2 + (1-d) T \frac{1}{2} (I_1 + I_2) \right] \quad (7)$$

$$i_{o',avg} = \frac{1}{T} \left[\frac{1}{2} I_2 t_1 - \frac{1}{2} I_1 t_2 + (1-d) T \frac{1}{2} (I_1 + I_2) \right] \quad (8)$$

A. Average Model

The average model can now be obtained from (2), (4) and (5), rewriting [15] the average currents as follows:

$$i_{i,avg} = \frac{(1-d)dTv_o}{nL_{lk}} \quad (9)$$

$$i_{o',avg} = \frac{(1-d)dTv_i}{L_{lk}} \quad (10)$$

Based on (6), the average model looks like in Fig. 3.

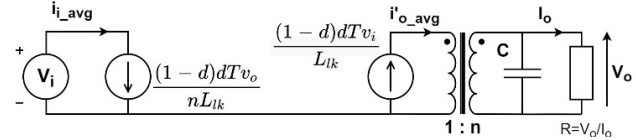


Figure 3. DAB converter average model

Using this model, the output voltage is expressed as a function of the input voltage and the load, as follows:

$$v_o = \frac{d(1-d)TRv_i}{nL_{lk}} \quad (11)$$

The power transferred between the primary-secondary is:

$$P_o = \frac{d(1-d)Tv_i v_o}{nL_{lk}} \quad (12)$$

Finally, from (7) the voltage transfer ratio as a function of the phase-shift between the primary and secondary bridges is obtained [16]:

$$M = \frac{v_o}{nv_i} = \frac{d(1-d)TR}{n^2 L_{lk}} = d(1-d)k \quad (13)$$

B. Small Signal Model

Perturbing (6), the equations of the average input and output currents, the small signal model can be derived:

$$\hat{i}_{o',avg} = \frac{\partial i_{o',avg}}{\partial d} \bigg|_0 \hat{d} + \frac{\partial i_{o',avg}}{\partial v_i} \bigg|_0 \hat{v}_i = g_{od} \cdot \hat{d} + g_{ovi} \cdot \hat{v}_i \quad (14)$$

$$\hat{i}_{i,avg} = \frac{\partial i_{i,avg}}{\partial d} \bigg|_0 \hat{d} + \frac{\partial i_{i,avg}}{\partial v_o} \bigg|_0 \hat{v}_o = g_{id} \cdot \hat{d} + g_{ovo} \cdot \hat{v}_o$$

where g_{od} , g_{id} , g_{ovi} and g_{ovo} are:

$$g_{od} = \frac{v_i T (1-2D)}{nL_{lk}} = \frac{v_o (1-2D)}{(1-D)DR} \quad (15)$$

$$g_{id} = \frac{v_o T (1-2D)}{nL_{lk}} = \frac{v_o^2 (1-2D)}{v_i (1-D)DR} = \frac{v_o}{v_i} g_{od} \quad (16)$$

$$g_{ovi} = g_{ivo} = \frac{TD(1-D)}{nL_{lk}} = \frac{v_o}{v_i R} \quad (17)$$

Now, based on (10) the circuit schematic of the small signal model can be drawn, as in Fig. 4.

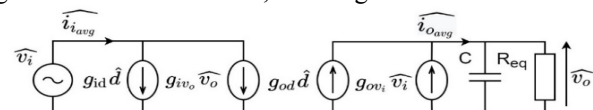


Figure 4. Small signal model of a DAB module

Based on the small signal model, the variations of the output voltage as a function of the input voltage and the phase-shift is:

$$\hat{v}_o = \frac{R}{RCs+1} (g_{od} \cdot \hat{d} + g_{ov_i} \cdot \hat{v}_i) \quad (14)$$

Substituting (11) and (13) into (14) and considering a constant input voltage, the transfer function can be obtained:

$$H_{DAB_o}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{v_i TR(1-2D)}{(RCs+1)2nL_{lk}} = \frac{v_o(1-2D)}{(1-D)D(RCs+1)} \quad (15)$$

Being a first order transfer function, a PI compensator with the following form is sufficient to achieve stability:

$$H_{PI}(s) = P + \frac{I}{s} = K \frac{1+sT}{sT} \quad (16)$$

where $I = \frac{K}{T}$; and $P = K$

C. PI Compensator Design

The mathematical model was implemented in Mathcad to produce an automated design sheet for the DAB converter modules. Fig. 5 is the plot of the obtained transfer function.

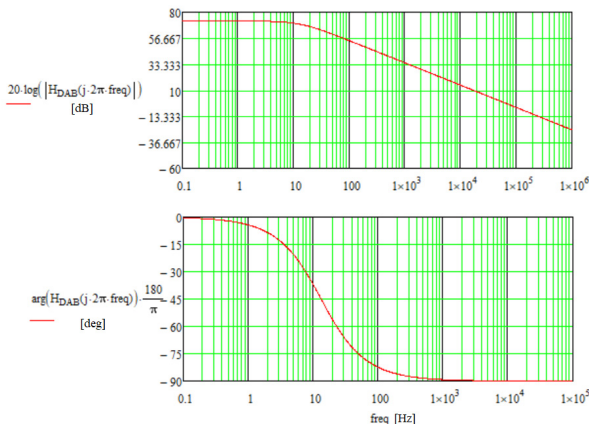


Figure 5. DAB module transfer function Bode plot and phase

Let the cutoff frequency f_c be tenth of the switching frequency f_{sw} , 1 kHz (in the case of using an f_{sw} of 10 kHz). Then at the frequency of 1 kHz:

$$|H_{DAB}(j\omega_c)| \cdot |H_{PI}(j\omega_c)| = 1, \text{ where } \omega_c = 2\pi f_c \quad (17)$$

Reading the plot of the transfer function from Fig. 5 at 1 kHz:

$$|H_{DAB}(j\omega_c)| = 34.5 \text{ dB} \rightarrow 53.1 \text{ rad} \quad (18)$$

$$\arg(H_{DAB}(j\omega_c)) = -89.24^\circ \rightarrow -1.5575$$

For stability and optimal functionality, the phase margin is chosen to be $\varphi_m = 70^\circ$. This means:

$$\arg(H_{DAB}(j\omega_c)) + \arg(H_{PI}(j\omega_c)) = -\pi + \varphi_m \quad (19)$$

$$\arg(H_{DAB}(j\omega_c)) + \arctan(\omega_c T) - \frac{\pi}{2} = -\pi + \varphi_m \quad (20)$$

From (20) the time constant from the PI's transfer function in (16) can be obtained as [17]:

$$T = \frac{\tan\left(\varphi_m - \frac{\pi}{2} - \arg(H_{DAB}(\omega_c))\right)}{\omega_c} = 4.2 \times 10^{-4} \text{ s} \quad (21)$$

Then from (17):

$$|H_{PI}(j\omega_c)| = \left| K \frac{1+j\omega_c T}{j\omega_c T} \right| = \frac{K\sqrt{1+\omega_c^2 T^2}}{\omega_c T} \quad (22)$$

From (22) K is obtained, which is the proportional constant:

$$K = \frac{\omega_c T}{|H_{DAB}(j\omega_c)| \cdot \sqrt{1+\omega_c^2 T^2}} = 0.018 = P \quad (23)$$

Having both K and T , the integral constant from (16) is now straightforward:

$$I = \frac{K}{T} = \frac{0.018}{4.2} 10^4 = 41.97 \approx 42 \quad (24)$$

Finally, the transfer function of the PI compensator is:

$$H_{PI}(s) = 0.018 + \frac{42}{s} \quad (25)$$

Parameter blocks for the PI design are also included in the automatized design sheet in Mathcad, as seen in Fig. 6.

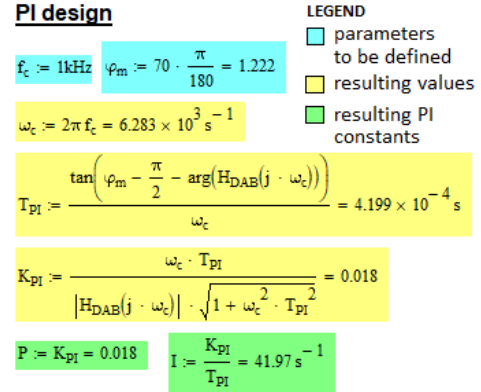


Figure 6. PI design sheet in Mathcad, where variables with blue are introduced values and yellow shows the resulting parameters

Plotting the compensated loop's transfer function in Mathcad, $H_c(s)$ – which is $H_{DAB}(s)$ multiplied by $H_{PI}(s)$ –, the design of the PI can be verified.

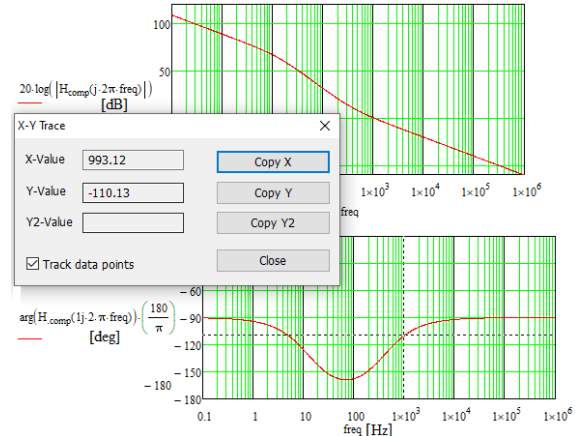


Figure 7. DAB module compensated transfer function Bode plot and phase (at crossover frequency)

As Fig. 7 shows, the phase margin is 70° . Applying Tustin or trapezoidal discretization on (25), the compensator's transfer function in Z domain is:

$$H_{PI}(z) = 0.018 + 42 \frac{T_s}{2} \frac{z+1}{z-1} \quad (26)$$

where T_s is a new variable, the sampling time or sampling period, usually lower than the switching period. Having a 10 kHz switching frequency, T_s will be $20 \cdot 10^{-6}$ s, which corresponds to 50 kHz. The transfer function in Z domain is:

$$H_{DAB_o}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{v_i TR(1-2D)}{(RCs+1)2nL_{lk}} \rightarrow$$

$$H_{DAB_o}(z) = \frac{(1+z^{-1})v_i TR(1-2D)}{\left[\left(1 + \frac{2RC}{T_s}\right) + \left(1 - \frac{2RC}{T_s}\right)z^{-1} \right] 2nL_{lk}} \quad (27)$$

Based on (26), the PI block configuration in Matlab/Simulink looks like in Fig. 8.

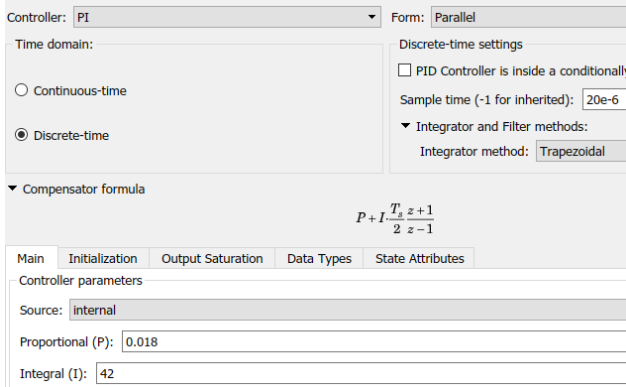


Figure 8. Simulink PI block configuration based on (26)

Simulation results of the PETT with DAB modules will be presented in Section 4.

III. DECOUPLED CONTROL STRATEGY OF THE MULTI-MODULAR TRACTION TRANSFORMER

Configuring power converters in modular ISOP connection is mostly used to achieve higher power density and power transfer. Using converters with the same parameters in each module simplifies their interconnection, however, balance problems can appear in the input voltage due to imperfections, parasitic quantities and other errors, even if they have the same component values, possibly leading to a voltage, current and inductance mismatch. This means, that the same control system operating each module will possibly lead to unbalanced voltage. On the other hand, the equations of the system show an interdependence between the electrical quantities of the converter and the control signals, moreover, the voltage distribution also depends on parasitic components. To illustrate this problem and present a solution, a PETT with four DAB modules is considered, as in Fig. 9. The converter bridges are operated with fixed duty cycle of 50% and the control variable is the phase shift between the primary and secondary side bridges. The proposed solution is the decoupling of control variables to obtain separate control loops for each module in a way that ZVS capability to be maintained [13].

Each bridge can be considered a dependent current source when modeling the ISOP connected converters. To obtain the model equations, the average input and output current equations were perturbed, as seen in section II.B. Then the total output current is the sum of each module's output:

$$\begin{cases} \hat{v}_o = \frac{R}{RCs+1} \hat{i}_o \\ \hat{i}_o = \hat{i}_{o1} + \hat{i}_{o2} + \hat{i}_{o3} + \hat{i}_{o4} \end{cases} \quad (28)$$

Then based on (6) \hat{v}_o is:

$$\hat{v}_o = \frac{R}{RCs+1} \cdot \left[g_{od} \cdot (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) + g_{ov_i} \cdot (\hat{v}_{i1} + \hat{v}_{i2} + \hat{v}_{i3} + \hat{v}_{i4}) \right] \quad (29)$$

When we consider the total input voltage to be constant, the sum of input voltages equals the total input voltage, so the term multiplying g_{ov_i} is zero. As a result, the equation becomes:

$$\hat{v}_o = \frac{R}{RCs+1} g_{od} (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) = G_{vd} (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) \quad (30)$$

where G_{vd} is the voltage-phase-shift gain. From the input port of each module the input currents are:

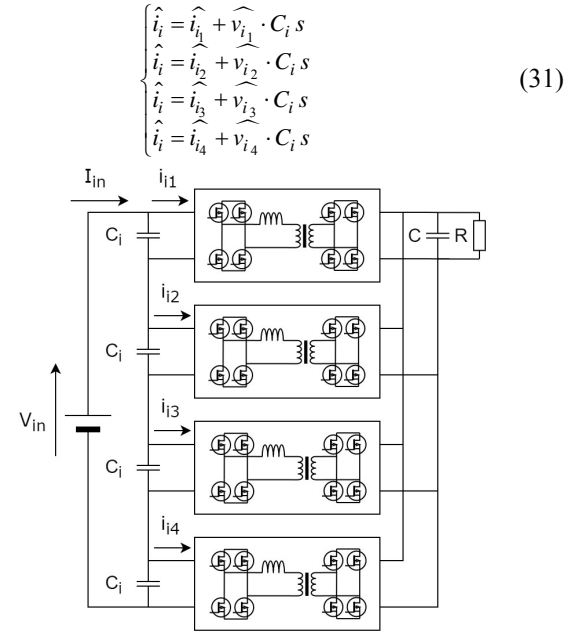


Figure 9. Eight modules DAB converter in ISOP connection

Adding the equations in (31) the expression of the total input current is found:

$$\hat{i}_i = \frac{1}{4} (\hat{i}_{i1} + \hat{i}_{i2} + \hat{i}_{i3} + \hat{i}_{i4}) + \frac{1}{4} (\hat{v}_{i1} + \hat{v}_{i2} + \hat{v}_{i3} + \hat{v}_{i4}) \cdot C_i s \quad (32)$$

In (32) the term $(\hat{v}_{i1} + \hat{v}_{i2} + \hat{v}_{i3} + \hat{v}_{i4})$ is 0 since the total input voltage is assumed to be constant, meaning that, based on (6), \hat{i}_i is:

$$\hat{i}_i = \frac{1}{4} [g_{id} (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) + 4 \cdot g_{iv_o} \cdot \hat{v}_o] \quad (33)$$

Substituting (30) into (33) \hat{i}_i finally is:

$$\begin{aligned} \hat{i}_i &= (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) \cdot \left(\frac{1}{4} \cdot g_{id} + g_{iv_o} \cdot G_{vd} \right) = \\ &= G_{ind} \cdot (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) \end{aligned} \quad (34)$$

where G_{ind} is a gain dependent on the converter parameters.

Considering (34) the input voltage for module one is:

$$\hat{v}_{i1} = \frac{\hat{i}_i - \hat{i}_{i1}}{C_i s} = \frac{1}{C_i s} [G_{ind} (\hat{d}_1 + \dots + \hat{d}_4) - (g_{id} \hat{d}_1 + g_{iv_o} \hat{v}_o)] \quad (35)$$

Substituting (30) into (35) \hat{v}_{i1} will be:

$$\hat{v}_{i1} = \frac{1}{C_i s} \cdot \left[G_{ind} \cdot (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) - g_{id} \cdot \hat{d}_1 - g_{iv_o} \cdot G_{vd} (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) \right] \quad (36)$$

Using G_{ind} from (34) the input voltage further developed:

$$\begin{aligned} \hat{v}_{i1} &= \frac{1}{C_i s} \left[(\hat{d}_1 + \dots + \hat{d}_4) \left(\frac{1}{4} g_{id} + g_{iv_o} G_{vd} - g_{iv_o} G_{vd} \right) - g_{id} \hat{d}_1 \right] \\ &= \frac{1}{C_i s} \left[\frac{1}{4} g_{id} (\hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4) - g_{id} \hat{d}_1 \right] \end{aligned} \quad (37)$$

The control strategy chosen for decoupling the variables is N-1 input voltages controlled by separate control loops and another loop for the output voltage (where N is the number of modules). To summarize the model equations a variable $A(s)$ is defined:

$$A(s) = \frac{g_{id}}{4C_i s} = \frac{1}{4C_i s} \frac{1}{L_{lk} \cdot n} V_o (1 - 2D) \quad (38)$$

Based on (36):

$$\begin{cases} \widehat{v_{i1}} = A(s) \cdot (\widehat{d_2} + \widehat{d_3} + \widehat{d_4} - 2 \cdot \widehat{d_1}) \\ \widehat{v_{i2}} = A(s) \cdot (\widehat{d_1} + \widehat{d_3} + \widehat{d_4} - 2 \cdot \widehat{d_2}) \\ \widehat{v_{i3}} = A(s) \cdot (\widehat{d_1} + \widehat{d_2} + \widehat{d_4} - 2 \cdot \widehat{d_3}) \end{cases} \quad (39)$$

Then using (37) and (28), the model equations can be summarized as:

$$\begin{bmatrix} \widehat{v_{i1}} \\ \widehat{v_{i2}} \\ \widehat{v_{i3}} \\ \widehat{v_o} \end{bmatrix} = \begin{bmatrix} -3A(s) & A(s) & A(s) & A(s) \\ A(s) & -3A(s) & A(s) & A(s) \\ A(s) & A(s) & -3A(s) & A(s) \\ G_{vd}(s) & G_{vd}(s) & G_{vd}(s) & G_{vd}(s) \end{bmatrix} \cdot \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \widehat{d_3} \\ \widehat{d_4} \end{bmatrix} = H(s) \cdot \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \widehat{d_3} \\ \widehat{d_4} \end{bmatrix} \quad (40)$$

In (40) can be noticed that the variation of normalized phase-shifts $\widehat{d_j}$ affects all the controlled quantities forming a multiple input, multiple output system from the modular converter. The system must be manipulated to consider each module a single input, single output system to avoid the interdependence of the quantities [13][18]. This can be achieved by applying the earlier mentioned control strategy. If the $H(s)$ matrix in (40) would be diagonal, each control signal will control a single quantity and each control quantity will depend on one signal only. Therefore, $H(s)$ is split into a diagonal matrix $D(s)$ and a transition matrix $Y(s)$:

$$H(s) = D(s) \cdot Y(s) = \begin{bmatrix} 4A(s) & 0 & 0 & 0 \\ 0 & 4A(s) & 0 & 0 \\ 0 & 0 & 4A(s) & 0 \\ 0 & 0 & 0 & 4G_{vd}(s) \end{bmatrix} \cdot Y(s) \quad (41)$$

Now the product of $Y(s)$ and the control variables will form a new set of control variables as follows:

$$\begin{bmatrix} \widehat{v_{i1}} \\ \widehat{v_{i2}} \\ \widehat{v_{i3}} \\ \widehat{v_o} \end{bmatrix} = \begin{bmatrix} 4A(s) & 0 & 0 & 0 \\ 0 & 4A(s) & 0 & 0 \\ 0 & 0 & 4A(s) & 0 \\ 0 & 0 & 0 & 4G_{vd}(s) \end{bmatrix} \cdot Y(s) \cdot \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \widehat{d_3} \\ \widehat{d_4} \end{bmatrix} = \begin{bmatrix} 4A(s) & 0 & 0 & 0 \\ 0 & 4A(s) & 0 & 0 \\ 0 & 0 & 4A(s) & 0 \\ 0 & 0 & 0 & 4G_{vd}(s) \end{bmatrix} \cdot \begin{bmatrix} \widehat{x_1} \\ \widehat{x_2} \\ \widehat{x_3} \\ \widehat{x_4} \end{bmatrix} \quad (42)$$

To see how the new set of control variables interacts with the original ones, $Y(s)$ and its inverse matrix must be computed to obtain the control variables $\widehat{d_i}$ as a function of the new control variables $\widehat{x_i}$.

$$Y(s) = D(s)^{-1} \cdot H(s) = \begin{bmatrix} \frac{1}{4A(s)} & 0 & 0 & 0 \\ 0 & \frac{1}{4A(s)} & 0 & 0 \\ 0 & 0 & \frac{1}{4A(s)} & 0 \\ 0 & 0 & 0 & \frac{1}{4G_{vd}(s)} \end{bmatrix} \cdot \begin{bmatrix} -3A(s) & A(s) & A(s) & A(s) \\ A(s) & -3A(s) & A(s) & A(s) \\ A(s) & A(s) & -3A(s) & A(s) \\ G_{vd}(s) & G_{vd}(s) & G_{vd}(s) & G_{vd}(s) \end{bmatrix} \quad (43)$$

$$Y(s) = \begin{bmatrix} -\frac{3}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & -\frac{3}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & -\frac{3}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \end{bmatrix} \quad (44)$$

Since this matrix is larger, its inverse matrix will be computed with the formula below:

$$Y(s)^{-1} = \frac{1}{\det(Y(s))} \cdot \text{adj}(Y(s)) \quad (45)$$

Now the determinant and the adjunct matrices will be calculated.

$$\det(Y(s)) = \begin{vmatrix} -\frac{3}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & -\frac{3}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & -\frac{3}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \end{vmatrix} \xrightarrow{C_1+3 \cdot C_2, C_3-C_2, C_4-C_2} \begin{vmatrix} 0 & \frac{1}{4} & 0 & 0 \\ -2 & -\frac{3}{4} & 1 & 1 \\ 1 & \frac{1}{4} & -1 & 0 \\ 1 & \frac{1}{4} & 0 & 0 \end{vmatrix} \xrightarrow{\text{expanding along row 1}} -\frac{1}{4} \begin{vmatrix} -2 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 0 & 0 \end{vmatrix} \xrightarrow{\text{expanding along row 3}} -\frac{1}{4} \begin{vmatrix} 1 & 1 \\ -1 & 0 \end{vmatrix} = -\frac{1}{4} \quad (46)$$

The adjunct matrix is the transposed cofactor matrix of $Y(s)$.

$$\text{adj}(Y(s)) = C_{Y(s)}^T = \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C_{34} \\ C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}^T \quad (47)$$

Then each element is calculated to fill the cofactor matrix.

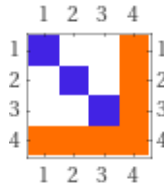
$$C_{11} = \begin{vmatrix} -\frac{3}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & -\frac{3}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & -\frac{3}{4} \end{vmatrix} \xrightarrow{C_1+3 \cdot C_2, C_3-C_2} \begin{vmatrix} 0 & \frac{1}{4} & 0 \\ -2 & -\frac{3}{4} & 1 \\ 1 & \frac{1}{4} & 0 \end{vmatrix} \xrightarrow{\text{expanding along row 1}} -\frac{1}{4} \begin{vmatrix} -2 & 1 \\ 1 & 0 \end{vmatrix} = \left(-\frac{1}{4}\right)(-1) = \frac{1}{4} \quad (48)$$

$$C_{12} = -\begin{vmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & -\frac{3}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & -\frac{3}{4} \end{vmatrix} = 0 \quad (49)$$

In the same way, the remaining elements are calculated to obtain the cofactor matrix of $Y(s)$, which is:

$$C_{Y(s)} = \begin{bmatrix} \frac{1}{4} & 0 & 0 & -\frac{1}{4} \\ 0 & \frac{1}{4} & 0 & -\frac{1}{4} \\ 0 & 0 & \frac{1}{4} & -\frac{1}{4} \\ -\frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} & \frac{1}{4} \end{bmatrix} \quad (50)$$

$Y(s)^{-1}$ and its co-factor matrix have the matrix plot in Fig. 10, which points to a general pattern that could be deduced for an n times n matrix for a system of N modules in ISOP configuration.

Figure 10. Matrix plot of the cofactor matrix of $Y(s)$

Having a matrix plot as in Fig.10, its transposed matrix is the same, therefore the adjunct matrix of $Y(s)$ is:

$$\text{adj}(Y(s)) = C_{Y(s)}^T = \begin{bmatrix} 1 & 0 & 0 & -\frac{1}{4} \\ 0 & 1 & 0 & -\frac{1}{4} \\ 0 & 0 & 1 & -\frac{1}{4} \\ -\frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} & 1 \end{bmatrix} \quad (51)$$

Finally, the inverse matrix of $Y(s)$ replacing the determinant and adjunct matrix is:

$$Y(s)^{-1} = \frac{1}{\det(Y(s))} \cdot \text{adj}(Y(s)) = \frac{1}{-\frac{1}{4}} \begin{bmatrix} 1 & 0 & 0 & -\frac{1}{4} \\ 0 & 1 & 0 & -\frac{1}{4} \\ 0 & 0 & 1 & -\frac{1}{4} \\ -\frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} & 1 \end{bmatrix} = \begin{bmatrix} -1 & 0 & 0 & 1 \\ 0 & -1 & 0 & 1 \\ 0 & 0 & -1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \quad (52)$$

As the final step the normalized time shifts (\hat{d}_i) are calculated from the new set of variables (\hat{x}_i).

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \\ \hat{d}_4 \end{bmatrix} = Y(s)^{-1} \cdot \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{x}_3 \\ \hat{x}_4 \end{bmatrix} = \begin{bmatrix} -1 & 0 & 0 & 1 \\ 0 & -1 & 0 & 1 \\ 0 & 0 & -1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{x}_3 \\ \hat{x}_4 \end{bmatrix} = \begin{bmatrix} \hat{x}_4 - \hat{x}_1 \\ \hat{x}_4 - \hat{x}_2 \\ \hat{x}_4 - \hat{x}_3 \\ \hat{x}_1 + \hat{x}_2 + \hat{x}_3 + \hat{x}_4 \end{bmatrix} \quad (53)$$

This result means, that for a 4 module system the decoupled control can be designed as seen in Fig. 11, where $\hat{d}_1 = \hat{x}_4 - \hat{x}_1$, $\hat{d}_2 = \hat{x}_4 - \hat{x}_2$, and $\hat{d}_3 = \hat{x}_4 - \hat{x}_3$ and $\hat{d}_4 = \hat{x}_1 + \hat{x}_2 + \hat{x}_3 + \hat{x}_4$.

In the previous section, the output voltage to normalized time-shift transfer function was deduced. However, decoupling the control loop, now the transfer function of the input voltage to normalized time-shift is also necessary, to calculate the PI compensator coefficients of C_1 to C_{N-1} , as seen in Fig. 11.

Starting from (10), the transfer function can be deduced:

$$\hat{i}_i = g_{id} \cdot \hat{d} + g_{ivo} \cdot \hat{v}_o \quad (54)$$

Substituting \hat{v}_o from (14) into (54) and using (12) and (13) we obtain:

$$\hat{i}_i = g_{id} \cdot \hat{d} + \frac{v_o}{v_i R} \frac{R}{RCs+1} g_{id} \frac{v_i}{v_o} \cdot \hat{d} \quad (55)$$

Finally obtaining:

$$\hat{i}_i = g_{id} \cdot \hat{d} \left(1 + \frac{1}{RCs+1} \right) = \frac{v_o T(1-2D)}{nL_{lk}} \left(1 + \frac{1}{RCs+1} \right) \quad (56)$$

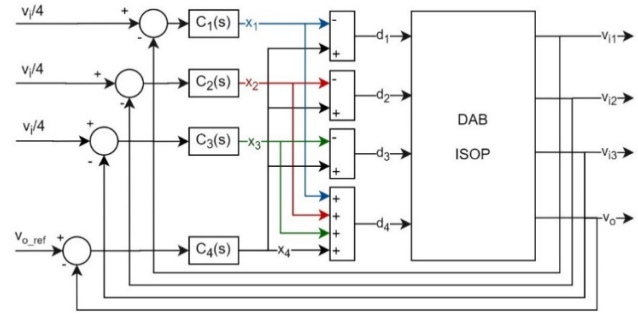


Figure 11. Control scheme of decoupled loops for implementation of a 4 modules system

Then the output voltage variation is:

$$\hat{v}_i = \frac{\hat{i}_i}{C_i s} = \frac{v_o T(1-2D)}{nL_{lk} C_i s} \left(1 + \frac{1}{RCs+1} \right) \cdot \hat{d} \quad (57)$$

From (57), the input voltage to normalized time-shift transfer function is:

$$H_{DAB_i}(s) = \frac{\hat{v}_i}{\hat{d}} = \frac{v_o T(1-2D)}{nL_{lk} C_i s} \left(1 + \frac{1}{RCs+1} \right) \quad (58)$$

Using (58), (16), the PI regulator's design equations (21) and (23), the PI regulator for the input voltage to normalized time-shift transfer function can be designed in the same way as for the output to normalized time shift transfer function. Fig. 12 shows the input voltage to normalized time-shift and its argument:

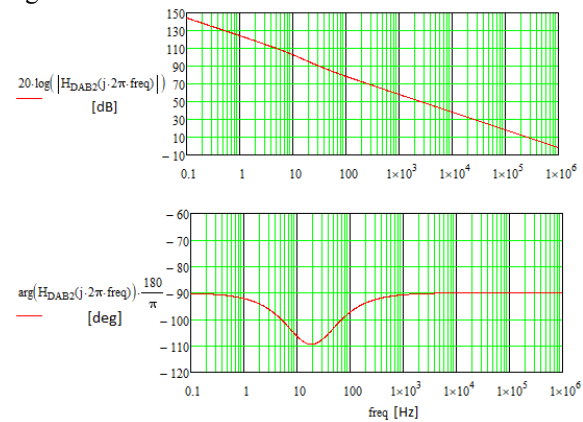


Figure 12. Transfer function of the input voltage to normalized time-shift and its phase

The automated Mathcad design sheet shown in Fig. 6 then calculates the parameters of the PI compensators C_1 to C_{N-1} (which use input voltage as a reference). Different parameters, as well as equations, can be defined in Mathcad, allowing a quick and easy way to obtain design parameters that are dependent on the designer's input as well as other complex equations and plots resulting from those inputs. The parameters can be colored differently depending on their role – input, output, or any other definition – to make the design process easier. Similarly to the blocks of parameters from Fig. 6, a group parameters were defined for compensators C_1 to C_{N-1} , see the results of the compensated transfer function on Fig. 13.

Based on the equations of the four modules system, the general equations for an N modules system can now be defined as the following equations (59)-(69).

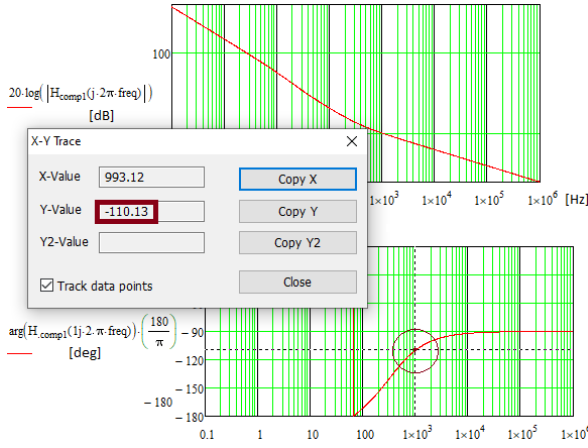


Figure 13. The 70° phase margin obtained with P and I of 0.00125 and 27.3 respectively

$$\hat{v}_o = \frac{R}{RCs+1} \cdot g_{od} \cdot (\hat{d}_1 + \hat{d}_2 + \dots + \hat{d}_N) = G_{vd} \cdot (\hat{d}_1 + \hat{d}_2 + \dots + \hat{d}_N) \quad (59)$$

$$\hat{v}_{ij} = \frac{1}{C_i s} \cdot \left[\frac{1}{N} \cdot g_{id} \cdot (\hat{d}_1 + \hat{d}_2 + \dots + \hat{d}_N) - g_{id} \cdot \hat{d}_j \right] \quad (60)$$

$$\hat{i}_i = (\hat{d}_1 + \hat{d}_2 + \dots + \hat{d}_N) \cdot \left(\frac{1}{N} \cdot g_{id} + g_{ivo} \cdot G_{vd} \right) = G_{ind} \cdot (\hat{d}_1 + \hat{d}_2 + \dots + \hat{d}_N) \quad (61)$$

$$A(s) = \frac{g_{id}}{NC_i s} = \frac{1}{NC_i s} \frac{1}{L_{lk} \cdot n} V_o (1-2D) \quad (62)$$

$$\begin{bmatrix} \hat{v}_{i1} \\ \vdots \\ \hat{v}_{iN-1} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} -(N-1)A(s) & \dots & A(s) & A(s) \\ \vdots & \ddots & \vdots & \vdots \\ A(s) & \dots & -(N-1)A(s) & A(s) \\ G_{vd}(s) & \dots & G_{vd}(s) & G_{vd}(s) \end{bmatrix} \cdot \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \vdots \\ \hat{d}_N \end{bmatrix} \quad (63)$$

$$= H(s) \cdot \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \vdots \\ \hat{d}_N \end{bmatrix}$$

$$H(s) = D(s) \cdot Y(s) = \begin{bmatrix} NA(s) & 0 & \dots & 0 \\ 0 & NA(s) & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & NG_{vd}(s) \end{bmatrix} \cdot Y(s) = \begin{bmatrix} NA(s) & 0 & \dots & 0 \\ 0 & NA(s) & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & NG_{vd}(s) \end{bmatrix} \cdot \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \vdots \\ \hat{x}_N \end{bmatrix} \quad (64)$$

$$Y(s) = D(s)^{-1} \cdot H(s) = \begin{bmatrix} -\frac{N-1}{N} & \dots & \frac{1}{N} & \frac{1}{N} \\ \vdots & \ddots & \vdots & \vdots \\ \frac{1}{N} & \dots & -\frac{N-1}{N} & \frac{1}{N} \\ \frac{1}{N} & \dots & \frac{1}{N} & \frac{1}{N} \end{bmatrix} \quad (65)$$

Having this form for $Y_{n \times n}(s)$ means that its determinant and adjunct matrix in general will be as in (66) and (67):

$$\det(Y(s)) = \frac{(-1)^{N-1}}{N} \quad (66)$$

$$\text{adj}(Y(s)) = \begin{bmatrix} \frac{(-1)^N}{N} & \dots & 0 & \frac{(-1)^{N-1}}{N} \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \dots & \frac{(-1)^N}{N} & \frac{(-1)^{N-1}}{N} \\ \frac{(-1)^{N-1}}{N} & \dots & \frac{(-1)^{N-1}}{N} & \frac{(-1)^{N-1}}{N} \end{bmatrix} \quad (67)$$

Then, the inverse matrix of $Y(s)$ in general will be:

$$Y(s)^{-1} = \frac{\text{adj}(Y(s))}{\det(Y(s))} = \begin{bmatrix} \frac{(-1)^N}{N} & \dots & 0 & \frac{(-1)^{N-1}}{N} \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \dots & \frac{(-1)^N}{N} & \frac{(-1)^{N-1}}{N} \\ \frac{(-1)^{N-1}}{N} & \dots & \frac{(-1)^{N-1}}{N} & \frac{(-1)^{N-1}}{N} \end{bmatrix} = \begin{bmatrix} -1 & \dots & 0 & 1 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \dots & -1 & 1 \\ 1 & \dots & 1 & 1 \end{bmatrix} \quad (68)$$

Finally, the time shift variables as a function of the new control variables will have the general form:

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \vdots \\ \hat{d}_N \end{bmatrix} = Y(s)^{-1} \cdot \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \vdots \\ \hat{x}_N \end{bmatrix} = \begin{bmatrix} -1 & \dots & 0 & 1 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \dots & -1 & 1 \\ 1 & \dots & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \vdots \\ \hat{x}_N \end{bmatrix} = \begin{bmatrix} \hat{x}_N - \hat{x}_1 \\ \vdots \\ \hat{x}_N - \hat{x}_{N-1} \\ \hat{x}_1 + \dots + \hat{x}_N \end{bmatrix} \quad (69)$$

IV. SIMULATION MODEL

The MVDC PETT designed is an eight-module system capable of 1.2 MW of total power (or more, depending on the design); with 25 kV input voltage (3125 V input voltage on each module), 1500 V output voltage and 10 kHz switching frequency. Fig. 15 presents the whole system consisting of Simulink blocks with the control loops block, the PETT and the traction inverter and motor, which are also highlighted on the figure.

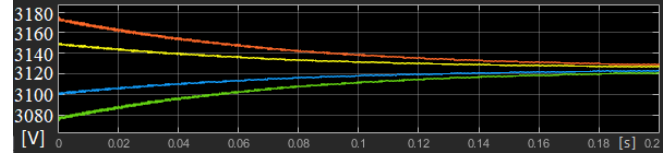


Figure 14. Different module input voltages balancing out

The PETT block contains eight DAB converters and the control block the PWM modulators. Fig. 14 illustrates how the input voltages of modules balances out in an ISOP controlled system. The compensator block is a simple PI controllers, since the transfer function of the system is first order. Fig. 16 represents the leakage inductor current and voltage, and the primary voltage. As it can be noticed, I_L and V_L have the same form as in Fig. 2 from II. On Fig. 17 the output voltage and current is shown. The output of the system reaches stability in less than five milliseconds and the output voltage ripple is negligible (less than 10% in any case). On Fig. 18 the whole range of possible input voltage variation is covered (steps between 19 kV – 27 kV, the lowest and highest non-permanent voltage) and the output voltage and total power can be seen as being 1500V and 1.2 MW respectively. Fig. 19 shows some load steps – different amount of power being drawn. The controller reacts fast and keeps constant the controlled variables at each step.

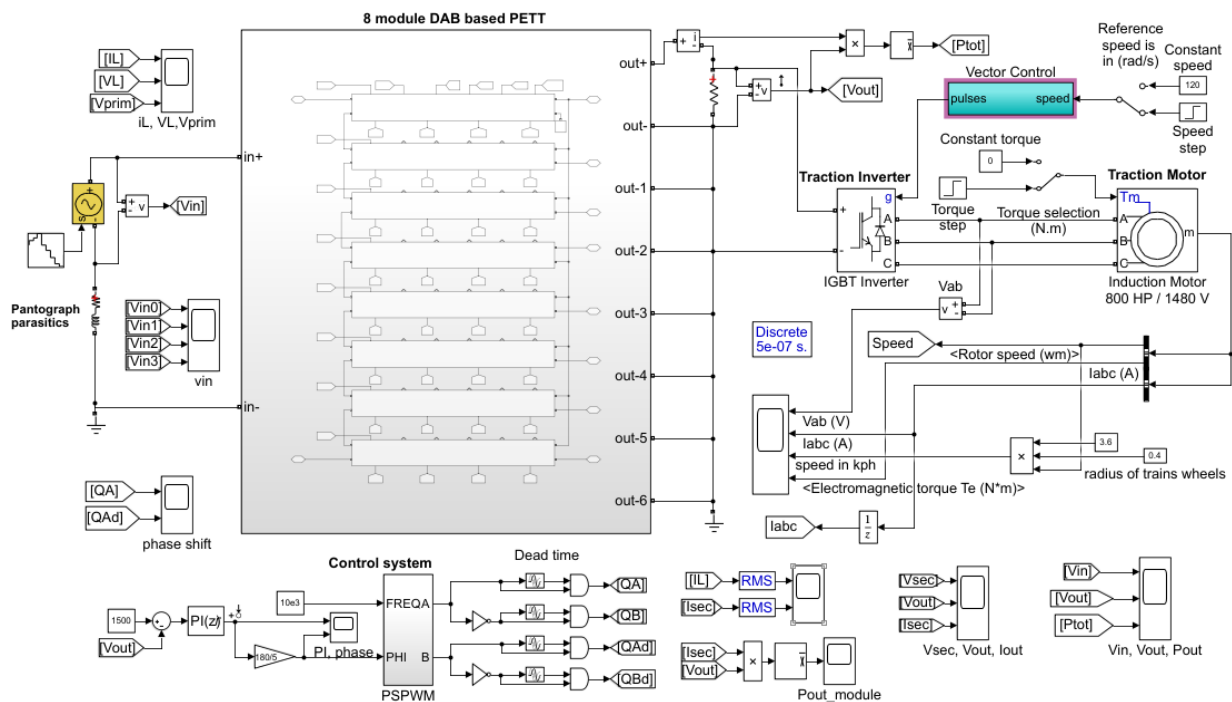


Figure 15. The simulation model of the 8-module power electronic traction transformer with pantograph parasitic and input voltage variations



Figure 16. Primary waveforms

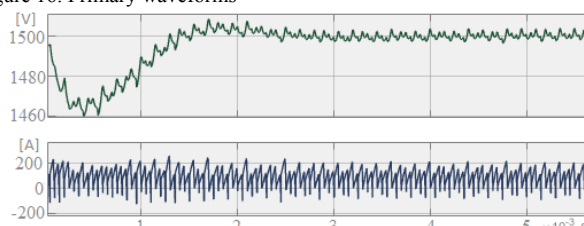


Figure 17. Output voltage and current

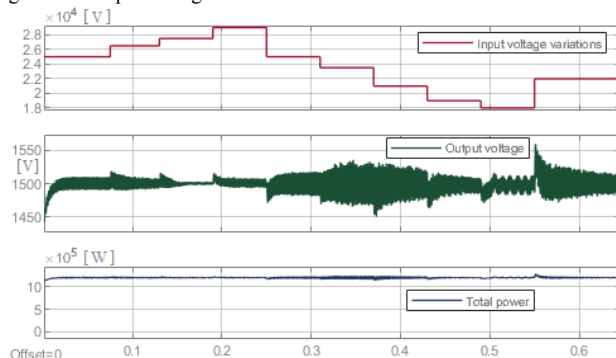


Figure 18. Ten different voltage levels – the catenary voltage range

Finally, the motor waveforms are presented on Fig. 20, showing an acceleration and a torque step of the locomotive.

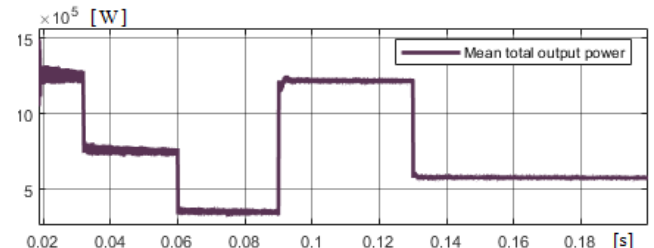


Figure 19. Total output power of the PETT: Maximum power and different load steps

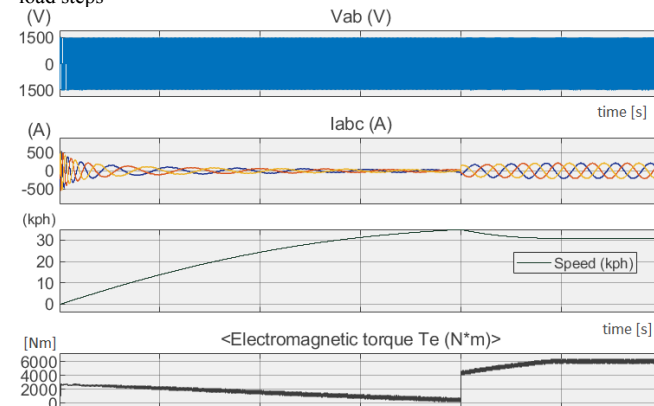


Figure 20. Voltage on motor, three phased current, speed and torque steps

A. Considerations on WBG Semiconductors

As Silicon (Si) semiconductors have already reached their full potential, a new generation of semiconductors and switching devices, using new WBG materials, have been emerged to replace Si devices. Such WBG semiconductors are: SiC, Gallium Nitride (GaN) and diamond. They are used to develop IGBTs, MOSFETs, thyristors, JFETs, GTOs, BJTs and power diodes, which significantly improve the performance of power converters. GaN and SiC are currently the most mature among WBG semiconductors, therefore in here only these two will be discussed.

Although GaN can achieve higher frequency and voltage, due to the lack of good bulk substrates and lower thermal conductivity, currently SiC is more promising. Some

achievements in SiC technology include: bulk material growth, advances in SiC wafers, larger dielectric critical field, meaning a ten times higher blocking voltage for the same thickness [19].

Commercial Si IGBTs are limited to a blocking voltage of 6.5 kV and temperature of 200 °C (which implies complex and expensive cooling sometimes) in comparison to SiC devices, which have much higher thermal conductivity and can operate even above 300-400 °C with a melting point of 3000 °C [19]. Therefore, when considering the usage of Si devices it must be taken into account the necessity of a large number of series connected switches in PETT systems, since they are modular multi-level with high voltage on front-end converters. This also implies special gate drives and increased complexity of control. This issue has been addressed by development of high voltage WBG switches like 10 kV and 15 kV SiC IGBTs and MOSFETs. In addition, the WBG semiconductors enable the converters to operate at higher switching frequency (up to 100 kHz) while maintaining high energy efficiency. This decreases the size and weight of passive filters and heat-removal system and in consequence, increases the power density of the converters.

When discussing about high voltage semiconductors it must be noted however, that the resistance of the ideal drift region can be related to the basic properties of the semiconductor material. It was demonstrated in [20], that the specific resistance of the ideal drift region can be obtained as:

$$R_{on-ideal} = \frac{4BV^2}{\epsilon_s \mu_n E_c^3} \quad (70)$$

In equation (70) the denominator is referred to as “Baliga’s figure of merit for power devices” and indicates the impact of material properties on the resistance of the drift region of a semiconductor. The cubic dependence on the critical electric field for breakdown of the on-resistance favors WBG semiconductors such as silicon carbide; however, the dependence of this resistance on the square of the breakdown voltage would affect the losses on semiconductors if too high voltage SiC devices were chosen in an application. R_{on} being directly proportional to BV^2 means that, for example, two 6.5 kV SiC devices in series would be more efficient than a single 10kV or 15 kV SiC device in term of power losses because of the on-resistance (since P is proportional with R). Therefore, in an application like MVDC-ERS probably the cost and power density gain will decide on the choice of voltage of the semiconductors.

SiC Schottky diodes have been commercialized since 2001 already and they are used in IGBT power modules too as freewheeling diodes. These IGBTs are known as Si-SiC hybrid semiconductors and Japanese railways have reported a 60% reduction in traction converter mass and volume [21]. Mitsubishi Electric also introduced SiC-only traction inverters for the Japan-Tokyo 1.5 kV DC metro in 2015, resulting in a 30% reduction in energy consumption and a 55% reduction in power loss [22]. Two years later, in [23] the first traction system for high-speed trains was reported based on SiC devices combined with train-draft cooling system and a new series of 6-pole induction motors. Thanks to SiC technology, the main transformer and the conversion system could be installed in the same car due to

compactness and to the 10% smaller new motors; an overall system weight reduction of 20% was achieved compared to the previous series of the train. In [24] a PETT was presented built with the earlier mentioned junction barrier SiC diodes and 15 kV/120 A SiC MOSFETs. At one MVA power, the achieved efficiency was 98% and the weight reduction 70%. A SiC MOSFET traction inverter was also operated in the Stockholm Metro System for 3 months and showed increased power density, achieving a reduction of 51% volume and 22% weight [25].

According to [19] SiC devices are developed for a large variety of applications and voltage ranges starting from JFETs, junction barrier diodes, IGBTs, MOSFETs and BJTs to SiC-GTOs. However, some of these devices are not as mature as others due to reliability problems. Theoretical studies show that SiC MOSFETs are a good candidate up to a 10-15 kV breakdown voltage, while IGBTs are the devices with the highest potential for applications above 15 kV, due to their very good on-state performances. In [26] a 27 kV SiC IGBT was reported as laboratory experiment and [27] mentions an engineering sample of a SiC GTO of 22 kV.

Paper [27] presents a survey on recent advances of MV SiC power devices. Beside the already mentioned advantages of SiC devices, it mentions some reports about lower on-state resistance, switching energy and cooling requirements. However, higher voltage ratings and switching frequencies imply challenges in the packaging. To avoid overshoots and current imbalances, the packaging must have low parasitic capacitance and inductance. In [28] a 57% loop inductance reduction was achieved only by adding decoupling capacitors inside the MOSFET module and [29] also reports such inductance reduction by doing different tests without and with decoupling capacitors. A stacked substrate structure that improves not only the parasitic capacitance reduction but thermal performance as well was also presented in [28]. The smaller dimensions of SiC devices brings also insulation issues, therefore [28] proposed a stacked insulation structure, reducing the strength of peak electric field by up to 40% compared to single substrates.

Regarding GaN devices, based on the review paper [30], they still have low availability, especially in high power domain. This is the main reason it was not discussed in more detail here. It should be also noted, that different reliability qualification standards will be necessary for GaN devices and compared to SiC devices GaN based power converter thermal design is critical and challenging, since thermal runaway occurs from both switching and conduction losses. GaN hetero-junction field effect transistors have more specific gate driver requirements and fewer gate driver ICs are on the market designed for the GaN device’s requirements. Drivers have to mitigate the cross-talk effect as well. Finally, currently, GaN device is more suitable for high-frequency applications in the MHz range.

V. CONCLUSIONS

In conclusion, the paper presented the detailed mathematical deduction of the DAB converter’s average and small signal model, as well as its connection in ISOP. The model shows, that the electrical quantities of the converters and the control signals are interdependent. Section III

presents in detail a controller, offering its scalable general form for N modules. Finally, in section IV the paper presents a fully functional traction transformer for the novel MVDC railway electrification system, including a short review on the impact of WBG semiconductors on the efficiency and design of a novel DC PETT system. This work developed a scalable multi-modular DC traction system and its controller design sheet and further work will include a small-scale experimental prototype of the system.

ACKNOWLEDGMENT

This project has received funding from the Shift2Rail Joint Undertaking (JU) under grant agreement No 826238. The JU receives support from the European Union's Horizon 2020 research and innovation programme and the Shift2Rail JU members other than the Union.

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