Stability Aspects in One-Cycle Controlled Buck Converters

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***Abstract*—The paper aims to investigate issues related to one cycle controlled buck converters stability, in the situation when the integration capacitor discharging is performed through a non-zero value resistor, as it happens in practice. It is known that in this case the exponential discharge makes capacitor voltage theoretically never reach zero. Under these conditions, instability phenomena are expected when the discharge time is short, that is at high duty cycles. The stability condition is analytically derived with respect to the control voltage. It is shown that instability occurs with period doubling leading to a half switching frequency subharmonic. Computer simulations confirm the validity of theoretical considerations.**

***Index Terms*—bifurcation, converter, one cycle control, simulation, stability.**

I. Introduction

One cycle control (OCC) technique was introduced by Smedley and Ćuk [1-2], and several models for it were proposed [3-4]. It has been a very promising control when applied to buck or Ćuk converters. This control technique was then extended by Lai and Smedley to the so called "integration control" [5-6] and applied to different switching converters [7-10].

Chaotic and bifurcation aspects related to dc-dc switching converters operating in different modes have been intensively reported [11-19]. As OCC principle assumes an inherent loop, it becomes natural that stability and eventually bifurcation and/or chaotic behavior to be investigated. Several attempts in this direction were made [20-22]. Most of them assumed ideal components, but operation with nonideal devices could also lead to instability when the converters are operated in peculiar regimes.

The OCC principle is illustrated in Fig. 1 when used in conjunction with a buck converter.

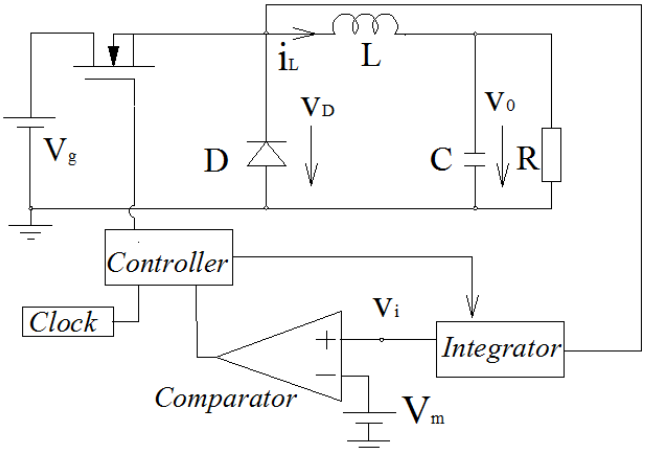

Figure 1. A buck converter employing one-cycle control.

A narrow pulse clock sets the constant switching frequency and determines the moments when the transistor is switched on. The same time the transistor starts to conduct the diode voltage is integrated till the threshold imposed by the control voltage is reached. When the integrator output voltage equals the control voltage the transistor is switched off for the rest of current switching cycle. When the threshold is reached also the integrator is reset.

It has been shown that converters using this technique reject input voltage perturbations in exactly one switching cycle and tightly follow the control reference very quickly. Therefore, the OCC technique is suitable for large-signal robust control of PWM switching converters, but also for quasi resonant converters or inverters and rectifiers as well. With capitals denoting dc values, transistor on time can be found solving the equation:

$$V_D = \frac{1}{T_s}\int_0^{dT_s} v_g(t)dt = v_m \tag{1}$$

where T_s is the switching period. However, in practice, the switches are not ideal and the integrator reset is not instantaneous. Therefore, the accuracy of OCC is greatly dependent upon circuit design.

II. Steady State Analysis of the OCC Controlled Buck Converter

A practical implementation for a buck converter with OCC, operating in CCM mode, is shown in Fig. 2.

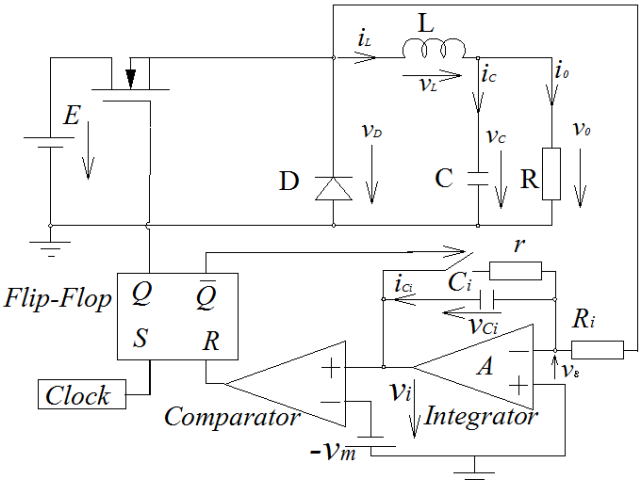

Figure 2. Practical implementation of an OCC controlled Buck converter.

Voltage variation across the integration capacitor in the two complementary topological states (t_{ON}, t_{OFF}) of the circuit active switch is shown in Fig. 3, assuming stable

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operation. With constant v_g, the absolute value of the voltage variation across the integration capacitor is linear and consistent with its charging law, as in equation (2).

$$v_{Ci}(t) = \frac{1}{C_i}\int_0^t \frac{V_g}{R_i}dt + V_{Ci(0)} \tag{2}$$

It is considered that, at the initial moment, the integration capacitor equals some nonzero value, $V_{Ci(0)}$, In Fig. 3, it corresponds to the increasing part, with a positive slope, from $V_{Ci(0)}$, to V_m:

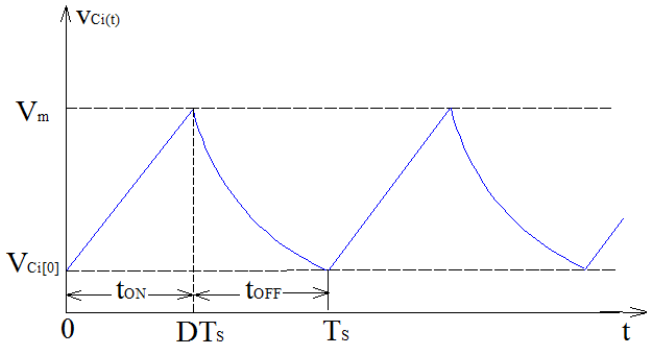

Figure 3. OCC Buck integration capacitor in steady state.

In steady state, the maximum value attainable by capacitor voltage is reached at the end of the conduction time of the transistor, that is after a time period equal to DT_s. On the other side, this value is equal to the control voltage V_m, as shown in equation (3):

$$V_m = \frac{1}{C_i}\int_o^{DT_s} \frac{V_g}{R_i}dt + V_{Ci(0)} \tag{3}$$

Expressing the integral in equation (3), we obtain:

$$V_m - V_{Ci(0)} = \frac{V_g T_s}{R_i C_i} D \tag{4}$$

From the OCC loop, when V_{Ci}=V_m, the Flip-Flop circuit switches off the transistor but also sends the control signal to close the switch in parallel to the integration capacitor C_i. Thus, the capacitor is discharged though resistor r according to an exponential discharge law. In practice this resistance is necessary in order not to have an excessive high discharge current through the discharge switch. In the second topological phase, when the transistor is off, the capacitor discharges according to the law given by equation (5), until this voltage, in a steady state, reaches again the value $V_{Ci}(0)$.

$$V_m e^{-\frac{(1-D)T_s}{rC_i}} = V_{Ci}(0) \tag{5}$$

This is the moment when the transistor is back into conduction and a new charging-discharging cycle starts.

Replacing (5) in (4) we obtain:

$$V_m - V_m e^{-\frac{(1-D)T_s}{rC_i}} = \frac{V_g T_s}{R_i C_i} D \tag{6}$$

On the other side, it is known that for the ideal buck converter the duty cycle is given by:

$$D = \frac{V_o}{V_g} \tag{7}$$

Substituting (7) into (6) and rearranging the terms, it follows that:

$$V_m = \frac{T_s}{R_i C_i}\frac{1}{1 - e^{-\left(1-\frac{V_o}{V_g}\right)\frac{T_s}{rC_i}}} V_o \tag{8}$$

Relationship (8) provides the correspondence between the control voltage V_m and the output voltage, as well as the switching period and the values of the circuit elements in the OCC loop.

To find a relationship between V_m and $V_{Ci}(0)$, we substitute the value of the duty cycle from equation (4) in equation (6), obtaining:

$$V_m e^{-\frac{Ts}{rC_i}+\frac{R_i}{r}\cdot\frac{[V_m - V_{Ci}(0)]}{V_g}} = V_{Ci}(0) \tag{9}$$

III. Analysis of the OCC Controlled Buck Converter in the Presence of Perturbations

In the analysis below the perturbations will be denoted by hatted variables. In the presence of a small perturbation in the control voltage, the integrating capacitor voltage changes from steady state as depicted in Fig. 4.

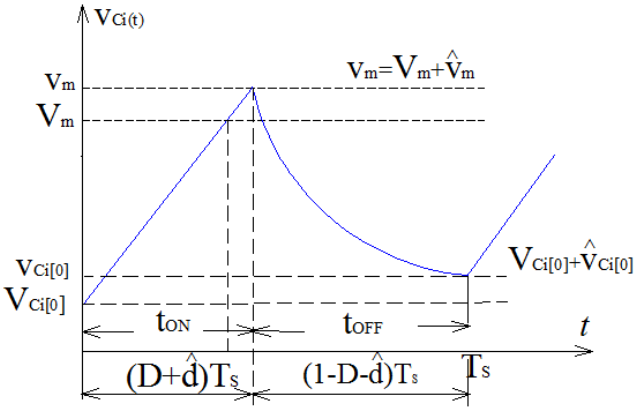

Figure 4. Capacitor C_i voltage in the presence of a small perturbation $\hat{v}_m$

With the perturbation applied, equations (3) and (5) modify as:

$$\begin{cases} V_m + \hat{v}_m = \dfrac{1}{C_i}\displaystyle\int_o^{(D+\hat{d})T_s} \frac{V_g}{R_i}dt + V_{Ci(0)} \\ (V_m + \hat{v}_m)e^{-\frac{(1-D-\hat{d})T_s}{rC_i}} = V_{Ci(0)} + \hat{v}_{Ci(0)} \end{cases} \tag{10}$$

Obviously, also the minimum capacitor value and the duty cycle will be perturbed, too, as equation (10) shows.

The first equation in (10) corresponds to the first topological state, when the transistor is on and the integration capacitor is linearly charged directly from the supply voltage until the ramp meets the perturbed reference voltage value, $V_m + \hat{v}_m$. The second equation in (10) is the equation describing the capacitor discharge while the transistor is blocked, until capacitor voltage reaches the value $V_{Ci}(0) + \hat{v}_{Ci}(0)$.

IV. OCC Buck Converter Discrete Equations in the Presence of Perturbations

Stability analysis can be carried out in discrete time with the index defined by the period number. The purpose is to determine the recurrence that exists between the integration capacitor voltage values at the beginning of two consecutive

periods: nT_s and $(n+1)T_s$. Referring to the waveforms enfaced in Fig. 5, we can write that:

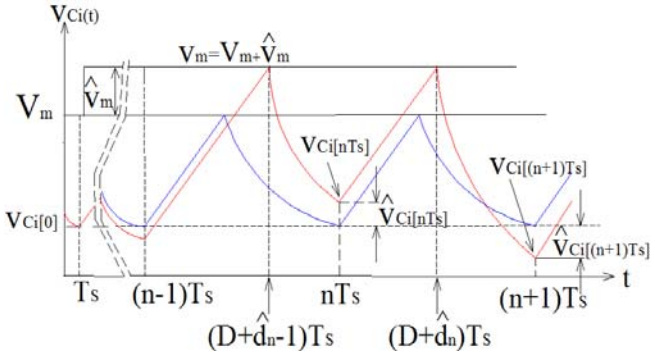

Figure 5. Waveforms after n+1 periods of PWM for the OCC Buck converter: unperturbed steady state (blue) and perturbed state (red)

$$\begin{cases} v_{Ci}(nT_s)+\dfrac{V_gT_s}{R_iC_i}d_n = v_m \\ v_m e^{-\frac{(1-d_n)T_S}{rC_i}} = v_{Ci}\left((n+1)T_s\right) \end{cases} \tag{11}$$

where

$$d_n = D+\hat{d}_n;\quad v_m = V_m+\hat{v}_m \tag{12}$$

Linearizing the equations in (11) around the operating point $v_m = V_m$, $d_n = D$, under small signal assumptions $\hat{v}_m << V_m$ and $\hat{d} << D$ and expressing $\hat{d}_n$ from the first linearized equation resulting from (11), after some algebra one obtains:

$$\begin{cases} \hat{d}_n = \dfrac{\left[\hat{v}_m-\hat{v}_{Ci}(nT_s)\right]R_iC_i}{V_gT_s} \\ \hat{v}_{Ci}\left((n+1)T_s\right) = e^{-\frac{(1-D)T_s}{rC_i}}\hat{v}_m + V_m\dfrac{T_S}{rC_i}e^{-\frac{(1-D)T_s}{rC_i}}\hat{d} \end{cases} \tag{13}$$

From the second equation in (13), it is clear that a dependency of the form:

$$\hat{v}_{Ci}\left((n+1)T_s\right) = f\left(\hat{v}_{Ci}(nT_s)\right) \tag{14}$$

will result substituting $\hat{d}_n$ from the first equation in the second one. After rearranging the terms, one obtains:

$$\hat{v}_{Ci}\left((n+1)T_s\right) = -\left(\frac{R_iV_m}{rV_g}e^{-\frac{(1-D)T_s}{rC_i}}\right)\hat{v}_{Ci}(nT_s)+ \\ +\left(1+\frac{R_iV_m}{rV_g}\right)\cdot e^{-\frac{(1-D)T_s}{rC_i}}\cdot\hat{v}_m \tag{15}$$

Recurrence (15) is of the type:

$$\hat{v}_{Ci}\left((n+1)T_s\right) = a\hat{v}_{Ci}(nT_s)+k\hat{v}_m \tag{16}$$

with a and k constants easily identified from (15).As the perturbation was assumed to be constant, we can define $b = k\hat{v}_m$, with b also a constant. Consequently, relationship (16) is in fact a sequence with the general term defined by the classical recurrence:

$$x_{n+1} = ax_n + b \tag{17}$$

with constant a and b.

It is known from calculus that the solution for the general term of the sequence is given by:

$$x_{n+1} = a^n x_1 + b\frac{a^n-1}{a-1} \tag{18}$$

Identifying a and b in (15), recurrence (18) becomes:

$$\hat{v}_{C_i}\left((n+1)T_s\right) = (-1)^n\left(\frac{R_iV_m}{rV_g}e^{-\frac{(1-D)T_s}{rC_i}}\right)^n\hat{v}_{Ci}(0)+ \\ \left(1+\frac{R_iV_m}{rV_g}\right)\hat{v}_m e^{-\frac{(1-D)T_s}{rC_i}}\frac{(-1)^n\left(\left(\frac{R_iV_m}{rV_g}\right)^n e^{-\frac{n(1-D)T_s}{rC_i}}\right)-1}{-\left(\frac{R_iV_m}{rV_g}e^{-\frac{(1-D)T_s}{rC_i}}\right)-1} \tag{19}$$

Equation (19) relates the value $\hat{v}_{Ci}\left(n+1\right)T_s\right)$, after $n+1$ periods, to the initial perturbation, $\hat{v}_{Ci}(0)$. It has to be remarked that there is a sign alternation for $\hat{v}_{Ci}(kT_s)$in consecutive periods. When instability will occur, then $\left|\hat{v}_{Ci}(kT_s)\right| < \left|\hat{v}_{Ci}((k+1)T_s)\right|$, as shown in Fig. 5.

V. OCC Buck Converter Stability Analysis

Taking (18) to the limit we have:

$$\lim_{n\to\infty}x_{n+1} = \lim_{n\to\infty}a^n x_1 + \lim_{n\to\infty}b\frac{a^n-1}{a-1} \tag{20}$$

Keeping in mind that x_n is a perturbation, in order to have a stable control the perturbation has to vanish in time. From the mathematical point of view this implies that $\lim_{n\to\infty}x_{n+1} = 0$. The sufficient condition to achieve this is $|a|<1$.

As a is the coefficient of $\hat{v}_{Ci}(0)$ from (19), the stability condition is:

$$\frac{R_i}{rV_g} < \frac{1}{V_m e^{-\frac{(1-D)T_s}{rC_i}}} \tag{21}$$

Highlighting the value of V_m in (21), the condition can be rewritten as:

$$V_m < \frac{rV_g}{R_i}e^{\frac{(1-D)T_s}{rC_i}} \tag{22}$$

Replacing the value of V_m from (8) into (22), the final form is found:

$$\frac{T_s}{rC_i}\frac{V_o}{V_g}\frac{1}{e^{\left(1-\frac{V_o}{V_g}\right)\frac{T_s}{rC_i}}-1} < 1 \tag{23}$$

Relationship (23) provides the general stability condition for the OCC Buck converter.

It is interesting to note that ideal operation when $r=0$ results as a peculiar case leading to unconditioned instability. Indeed, viewing the right hand side as a function of r and taking the limit with $r\to 0$, it is easy to prove using l'Hospital rule that

$$\lim_{\substack{r\to 0\\ r>0}} \frac{T_s}{rC_i}\frac{V_o}{V_g}\frac{1}{e^{\left(1-\frac{V_o}{V_g}\right)\frac{T_s}{rC_i}}-1} = 0 < 1 \tag{24}$$

and thus the stability condition is always fulfilled.

VI. Calculation of the Threshold Control Voltage V_M that Leads the OCC Buck Converter into Instability

This assumes the equal sign in relation (22), in order to find V_m at the limit between the stability and instability regions.

$$e^{-\frac{(1-D)T_s}{rC_i}} = \frac{rV_g}{R_iV_m} \tag{25}$$

Substituting the exponential from (25) in (6) it results that:

$$V_m\left(1-\frac{rV_g}{R_iV_m}\right) = \frac{T_s}{R_iC_i}DV_g \tag{26}$$

From (26) we can express the duty cycle D:

$$D = \frac{V_m}{V_g}\frac{R_iC_i}{T_s}\left(1-\frac{rV_g}{R_iV_m}\right) \tag{27}$$

Replacing the value of D from (27) in (25) and rearranging, we obtain:

$$e^{\frac{T_s}{rC_i}+1-\frac{R_i}{r}\frac{V_m}{V_g}} = \frac{R_iV_m}{rV_g} \tag{28}$$

Equation (28) is a transcendent equation that provides the value of the control voltage V_m that drives the converter into instability.

VII. Matlab Stability Analysis of the OCC Buck Converter

The purpose of this paragraph is to investigate when the stability condition is not fulfilled. To simplify the calculations we make the notations:

$$D = M = \frac{V_o}{V_g}, \quad \frac{T_s}{rC_i} = p \tag{29}$$

It is known that for the buck converter $0 \le M \le 1$ and $p \ge 5$, because in practice usually $rC_i << T_s$. With these notations equation (23) can be put in the form:

$$f(M,p) = \frac{pM}{e^{p(1-M)}-1} < 1 \tag{30}$$

We shall represent the function f given by (30) in Matlab, considering that M ranges between 0.01 and 0.99, while p is between 5 and 1000. The result is depicted in Fig. 6.

From Fig. 6, it can easily be noted that for high values of M, for example *0.8-0.99* and for small values of p, for example in the range *5-150*, the function values exceed unity and even reaches a maximum value of *96.7* (for the pair *M=0.99* and *p=5*). This aspect denotes high instability in the region where *f(M,p)>1*.

In conclusion, the OCC Buck converter is expected to become unstable in this area. We shall highlight and check this aspect by simulating it in a dedicated circuit simulation package in a distinct paragraph.

VIII. Control Voltage Calculation for the OCC Buck Converter Stability Limit

If we note:

$$\frac{R_iV_m}{rV_g} = y \tag{31}$$

then equation (28) becomes:

$$e^{\frac{T_s}{rC_i}+1-y} - y = 0 \tag{32}$$

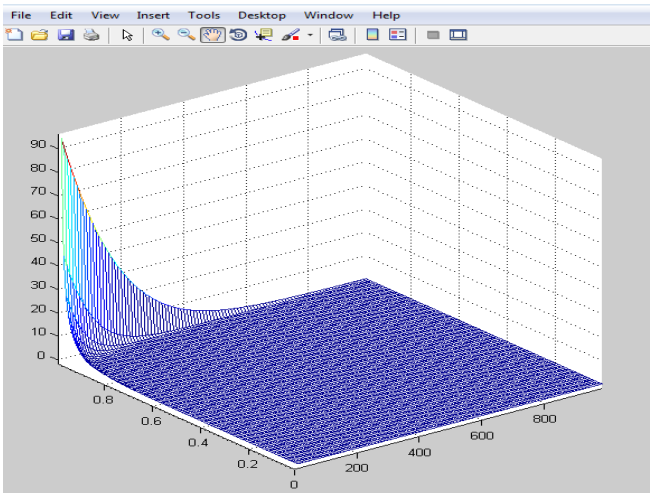

Figure 6. The 3D graph in Matlab for *f(M,p)*

Equation (32) is a transcendent equation that will be solved by numerical methods. Moreover, the equation has always a solution and this solution is unique because the function in y in the left hand side of (32) is monotonic, continuous and it takes values from $-\infty$ to $+\infty$.

As an example, we shall consider the buck converter with the following component values:

$R_i = 1k\Omega; C_i = 20nF; \quad f_s = 50kHz; V_g = 12V; V_o = 10V$,

$r = 66.67\Omega; \quad rC_i = 1.33\mu s$

Consequently, from (29) it results that $p = 15$ and $M = D = 0.833$.

Equation (32) is solved in Matlab and the solution is:

$$y = 13.3974 \tag{33}$$

from which the value of the control voltage is derived as:

$$V_m = y\frac{rV_g}{R_i} = 10.7178\ \text{V} \tag{34}$$

It is also interesting to represent the normalized dependency between M and the normalized control voltage V_m/V_g for the same converter. Under stable operation it is known that this dependency is the first bisector, but when instability occurs it will deviate from this. In order to draw the dependency of M against V_m/V_g, just divide (8) by V_g and make use of the previously defined notation, obtaining:

$$\frac{V_m}{V_g} = \frac{T_s}{R_iC_i}\frac{M}{1-e^{-p(1-M)}} \tag{35}$$

With fixed p, for each value of V_m the static conversion ratio is found by solving (35) and the results are presented in Fig.7 for three values of parameter *p={10,15,20}*.

To better see the output voltage deviation, we added the first bisector with a black trace and also performed a magnified view in the range *0.50-0.99* for V_m/V_g. It is

remarked that for values of M higher than *0.50*, the output voltage no longer follows the control voltage and for values of V_m close to V_g, the deviation V_m-V_0 has significantly high values. Also, the more p increases, the difference V_m-V_0 will also increase to higher values.

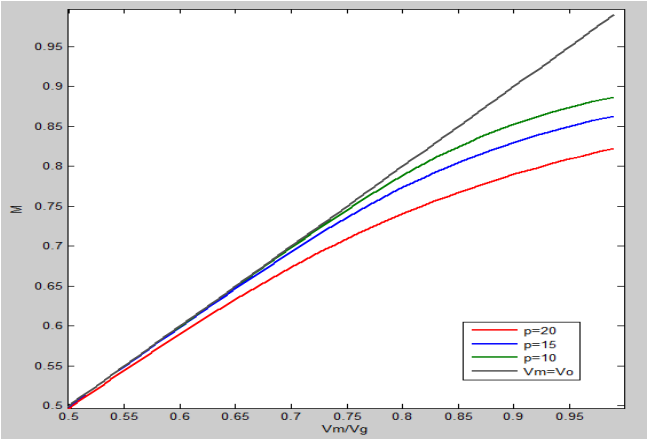

Figure 7. Static conversion ration against the normalized control voltage dependency: black trace– ideal dependency; colored traces – dependencies for different values of parameter p.

IX. Caspoc Simulation for the Buck Converter

The final validation will be performed by circuit simulation. The simulation schematic in Caspoc [23] is depicted in Fig. 8. The integrator was built using a 741 operational amplifier.

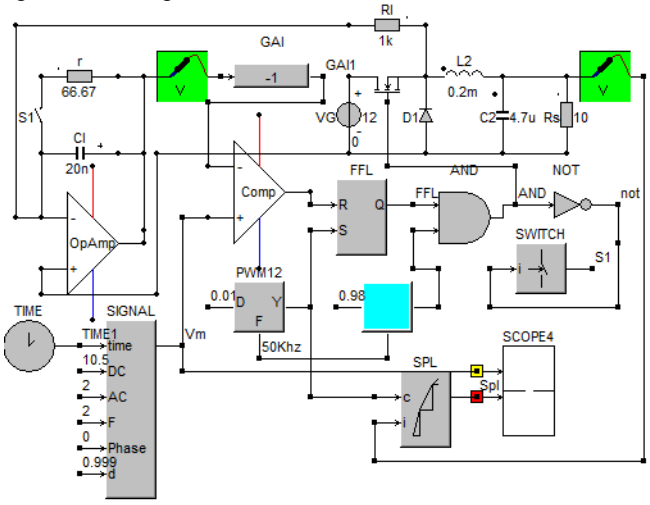

Figure 8. Simulation schematics of the buck converter with OCC.

First a stable operation was investigated corresponding to $D=M=8/12$ and $p=15$. The difference between V_0 and V_m was analytically calculated in Matlab and the result was $\Delta V = V_m - V_o = 46.8mV$. This result was compared and validated by Caspoc simulation as a difference of $46.6mV$ was found, that is with only 0.4% relative error.

Next the unstable operation was investigated choosing a control voltage V_m=*11V*, that is higher than the limit value *10.7178V* previously predicted. The results of the simulation are presented in Fig. 9.

Also the simulation confirms the unstable operation. Period doubling also brings an undesired increase in the output voltage ripple of *0.266V*, therefore almost double compared to stable operation without OCC in the same operating point.

Instability with the presence of a subharmonic leads to the idea that bifurcation phenomena are expected. This aspect will be detailed in section X.

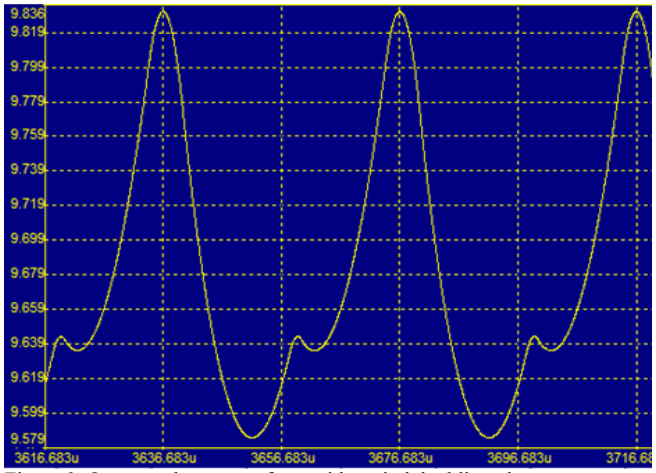

Figure 9. Output voltage waveform with period doubling phenomenon corresponding to V_m=*11V*, higher than the limit value

X. The Bifurcation Diagram Through Computer Simulation

In order to obtain the bifurcation diagram of the OCC controlled buck converter, the control voltage was very slowly varied between a minimum value, corresponding to stable operation, to an maximum corresponding to deep instability. As it can be seen in Fig. 8, the *2 Hz* parameter associated to the SIGNAL block showing that the control voltage is varied between the lower and upper limits in *0.5s*. This long time allows us to assume that the operation the converter passes a sequence of quasi steady states. The SPL block performs a sample and hold at a rate equal to the switching period, imposing that the value of the output voltage at exactly the beginning of the period will be displayed. On the other side, the simulation time step has to be chosen low enough compared to the switching period in order to perform accurate simulation during one switching cycle. Of course, the data were displayed corresponding to the time the control voltage is swept. Thus the simulation time step was dt=*5ns* and T_{Screen}=*400ms*. It can be seen that a very long simulation time is needed because the ratio between the screen length and the time step is quite high. In order to accelerate the simulation, data were displayed only at the beginning of each switching period as only the information at these time moments is needed. The bifurcation diagram is enfaced in Fig. 10.

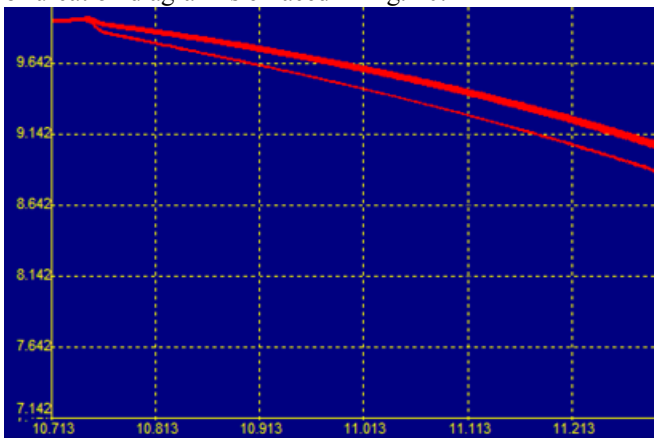

Figure 10. Bifurcation diagram for the OCC controlled buck converter.

It can be easily seen that bifurcation occurs at a value

V_m=*10.712V* corresponding to V_0=*9.925V* differing only by *5mV* and *2mV*, respectively, compared to the theoretically established values. This confirms the correctness of the theoretical considerations

XI. CONCLUSION

In spite of the fact that under ideal operation of the integrator the OCC controlled buck converter is always stable, when the capacitor is discharged through a nonzero resistance instability will always occur at high duty cycles and output voltages. The higher the discharge resistance the lower will be the limit value of the control voltage that marks the border between stable and unstable operation.

The limit value for the control voltage can be calculated and the theoretical results were accurately confirmed by simulations. It was shown that instability installs with a bifurcation phenomenon that significantly deviates the dc output voltage from the control voltage and leads to undesired higher voltage ripple.

Future research will focus on instability and eventually chaos behavior in OCC controlled fourth order converters.

REFERENCES

[1] K. M. Smedley, S. ´Cuk, "One-cycle control of switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, Nov. 1995, pp. 625-633.

[2] K. M. Smedley, S. ´Cuk, "Dynamics of one-cycle controlled Cuk converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, Nov. 1995, pp. 634-639.

[3] E. Santi, S. Cuk, "Modeling of one-cycle controlled switching converters," in Proc. 14th Int. Telecommunications Energy Conference, Washington, DC, 1992, pp. 131–138.

[4] N. Femia, M. Fortunato, G. Petrone, G. Spagnuolo, M. Vitelli, "Dynamic model of one-cycle control for converters operating in continuous and discontinuous conduction modes," *Int. J. Circuit Theory Appl.* vol. 37, issue 5, 2009, pp. 661–684.

[5] Z. Lai, K. M., Smedley, "A general constant-frequency pulsewidth modulator and its applications," *IEEE Trans. Circuits and Systems I: Fundam. Theory and Appl.*, vol. 45, no. 4, April 1998, pp. 386-396.

[6] Z. Lai, K. M., Smedley, "A family of continuous-conduction-mode power-factor controllers based on the general pulse-width modulator," *IEEE Trans. Power Electron*, vol. 13, no. 3, May 1998, pp. 501-510.

[7] Z. R. Lai, K. M. Smedley, "A new extension of one-cycle control and its application to switching power amplifiers," *IEEE Trans. Power Electron*, vol. 11, no. 1, Jan. 1996, pp. 99–105.

[8] D. Yang, M. Yang, X. Ruan, "One-cycle control for a double-input dc/dc converter," *IEEE Trans. Power Electron*, vol. 27, no. 11, Nov. 2012, pp. 4646-4655.

[9] D. Ma, "An integrated one-cycle control buck converter with adaptive output and dual loops for output error correction," *IEEE Journal of Solid-State Circuits*, vol. 39, issue 1, Jan. 2004, pp. 140-149.

[10] Quanming Luo, Shubo Zhi, Weiguo Lu, and Luowei Zhou, "Direct current control method based on one cycle controller for double-frequency buck converters," *Journal of Power Electronics*, vol. 12, no. 3, May, 2012, pp. 410-417.

[11] C. K. Tse, Complex Behavior of Switching Power Converters, 1st Edition, CRC Press, July 2003.

[12] E. R. Vilamitjana, A. E. Aroudi, E. Alarcón, Chaos in Switching Converters for Power Management, Springer, 2013.

[13] A. E. Aroudi, M. Debbat, R. Giral, G. Olivar, L. Benadero, E. Toribio, "Bifurcations in dc-dc switching converters: review of methods and applications," *Int. Journal of Bifurcation and Chaos*, 2005, vol. 15, issue 5, pp. 1549-1578.

[14] Z. T. Zhusubaliyev, E. A. Soukhoterin, E. Mosekilde, "Quasi-periodicity and border-collision bifurcations in a dc-dc converter with pulsewidth modulation," *IEEE Trans. Circuits and Systems-I: Fundam. Theory and Appl.*, vol. 50, issue 8, 2003, pp. 1047-1057.

[15] A. E. Aroudi, E. Rodriguez, R. Leyva, and E. Alarcon, "A design-oriented combined approach for bifurcation prediction in switched-mode power converters," *IEEE Trans. on Circuits and Systems-II: Express Briefs*, vol. 57, issue 3, 2010, pp. 218–222.

[16] M. Sattler, "Analysis of bifurcation behavior in power converters and the impact on the design process," in Proc. 11th IEEE Electric Ship Technologies Symposium (ESTS'11), Alexandria, VA, 2011, pp. 203–206.

[17] G. Podar, K. Chakrabarty, S. Banerjee, "Experimental control of chaotic behavior of buck converter," *IEEE Trans. Circuits and Systems-I: Fundam. Theory and Appl.*, vol. 42, issue 8, 1995, pp. 502-504.

[18] S. Maity, D. Tripathy, T. Bhattacharya, S. Banerjee, "Bifurcation analysis of PWM-1 voltage-mode-controlled buck converter using the exact discrete model," *IEEE Trans. on Circuits and Systems-I: Fundam. Theory and Appl.*, vol. 54, issue 5, 2007, pp. 1120–1130.

[19] M. Debbat, A. E. Aroudi, R. Bouyadjra, "Bifurcation analysis of current mode control Cuk dc-dc converter," *IEEE Trans. Circuits and Systems I: Fundam. Theory and Appl.*, vol. 55, no. 3, October 2012, pp. 20-25.

[20] W. Ma, M. Wang, C. Li, "Control of bifurcation in the one-cycle controlled Cuk converter," Springer, Nonlinear Dynamics [Online], March 2012, vol. 67, issue 4, pp 2573-2583. . [Online]. Available: http://link.springer.com/article/10.1007%2Fs11071-011-0170-8#page-1, DOI:10.1007/s11071-011-0170-8.

[21] M. Gurbina,, D. Lascu, "Unfeasibility of one cycle control when applied to zeta converters," *International Review of Automatic Control, Theory and Applications* , vol. 5, no. 2, March 2012, pp. 172-178.

[22] M. Gurbina, D. Lascu, "Analysis of one cycle controlled Sepic converter," in Proc. IEEE 8th International Symposium on Applied Computational Intelligence and Informatics (SACI), 2012, pp. 415-420.

[23] CASPOC, user manual . [Online]. Available: http://www.simulation-research.com/help/index.html.