# Phase-Synchronizer based on $g_m$–$C$ All–Pass Filter Chain

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***Abstract*—The use of analog CMOS circuits at high frequency has gained much attention in the last several years. At the heart of rapid prototyping of these circuits is the concept of using a versatile library of common RF function blocks. The blocks (cells) must be designed to be flexible in terms of drive requirements and loading. This paper presents the results of on-going research in development of phase-synchronizer as common RF function block, used in frequency and phase modulation, frequency synthesis, clock generation recovery, filtering, etc. The proposed circuit is based on series of voltage-controlled all-pass filter as delay chain, and enables phase regulation of analog input signals in wide range. Other characteristics of the input signal, such as amplitude and waveform are not deteriorated. The $g_m$–$C$ voltage-controlled all-pass filter is crucial block of the proposal. The IHP 0.25 μm SiGe BiCMOS technology was used for design and verification of the circuit. Simulation results indicate that it is possible to obtain phase regulation in the wide frequency range, from 100 kHz up to 200 MHz.**

***Index Terms*—RF circuits, all-pass filter, BiCMOS integrated circuits, $g_m$ –$C$ filter, phase control, tuned circuits.**

## I. INTRODUCTION

For correct operation of analog and digital circuits, both high-quality carrier and clock signals are needed. The main parameters of these signals are: stable frequency and phase, low noise, phase noise, jitter and clock-skew, as well as symmetrical duty-cycle. In order to fulfill design requirements all these parameters should be carefully taken into account. For example, the phase of analog signal often needs to be corrected without impact on other signal parameters, such as amplitude, waveform, etc. Phase synchronization of output signal in respect to the phase of reference input is common task in many applications [2-4].

Standard circuit for phase synchronization, known as a phase locked loop (PLL), is presented in Fig. 1(a). A phase of the voltage-controlled oscillator (VCO) is compared to the phase of reference input signal. If some error exists, it is eliminated by involving negative feedback. When PLL is in stable-state, the reference signal and VCO output are synchronized. Parameters of VCO output signal, such as amplitude and waveform, depend on VCO operation, itself [1]. In stable-state, other characteristics of the reference input signal (modulation, special waveforms) have not influence to VCO output.

In order to control the delay and synchronize clock timing in digital circuits, a delay locked loop (DLL), sketched in Fig. 1(b), is used. The clock signal passes through a chain of buffers, realized as voltage-controlled delay line (VCDL). The amount of delay depends on phase difference error between input and output VCDL signals. Steady-state is reached when these two clock signals are synchronized [2-4]. When the frequency multiplication is not used, DLL offers higher performances in respect to PLL, since its design is easier, and both the immunity to on-chip noise and stability of operation is much better [2], [4]. However, DLL circuit is based on VCDL, composed of buffers, designed only for processing digital clock signals. Having this in mind, it is not possible to achieve phase synchronization between two sinusoidal analog signals, by using DLL circuit.

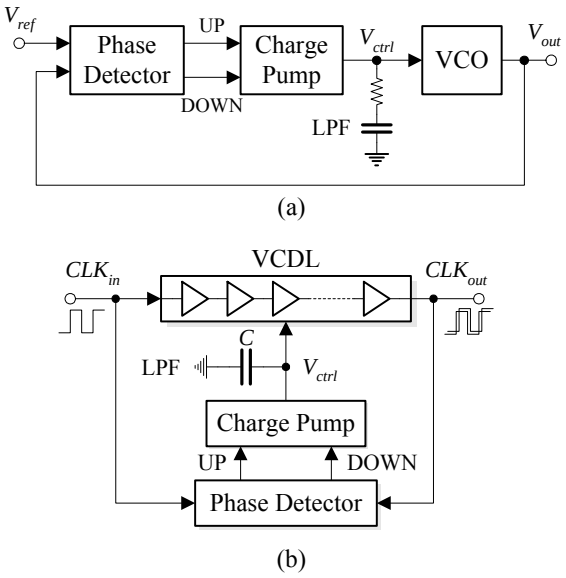


Figure 1. Block diagrams of PLL (a), and DLL (b)

Phase-synchronizer has become an integral part of many communication systems, as well as digital and control systems, and has found applications in diverse area such as, frequency and phase modulation, frequency synthesis, clock generation recovery, filtering, etc.

The main contribution of this paper is design of a phase-synchronizer based on series of voltage-controlled all-pass filter as a delay chain. Its operation is similar to DLL [16], [17]. In this proposal, VCDL is substituted with voltage-controlled $g_m$-$C$ all-pass filter (VCAPF) chain. This provides us to achieve phase correction of sinusoidal or some other complex periodical signals without violating the characteristics of reference signal. In comparison to DLL circuit, delay correction becomes now phase correction while all good properties of DLL, such as the first-order loop, stability and short settling time, are preserved.

Special attention is dedicated to design improvement of the VCAPF, as well as to verification of a design. Possible problems arising in phase loop control operation are described and, accordingly, corrective measures to prevent undesirable responses are proposed. The overall phase loop

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stability is proved on the basis of the Lyapunov control theory [15]. The proposed approach is suitable for the phase synchronization between two analog signals, as well as for generating multi-phase signals, quadrature signals, etc.

The paper is organized as follows. Section II concentrates on realization of the first-order $g_m$–$C$ all–pass filter. The structure of all–pass filter chain with phase loop control is defined and described in the Section III. Design solutions of phase detector, charge pump, low-pass filter and zero crossing detectors are also considered in details. Stability of the proposed phase loop is proved by using the Lyapunov stability theorem in Section IV. Simulation results are presented in Section V and applications examples in Section VI. Finally, Section VII contains some concluding remarks.

## II. VOLTAGE-CONTROLLED ALL–PASS FILTER

By using all-pass filters, without influence on signal amplitude, the phase of analog signal can be varied [6], [7], [17]. A scheme of the first-order all-pass filter is given in Fig. 2(a). In this case, the all-pass filter is realized as a continuous $g_m$–C filter [6]. An operational transconductance amplifier (OTA) and capacitors are used as filter constituents. In addition, an operational amplifier (OA) presented in Fig. 2(a), is used as non-inverting amplifier with unity gain. Due to large input impedance, its role is to prevent the influence of load impedance $Z_L$ on filter transfer function.

By substituting OTA with transconductance $g_m$, we obtain the equivalent electrical model presented in Fig. 2(b). Since OA has no influence on transfer characteristic of the filter, it is omitted in the equivalent electrical scheme.

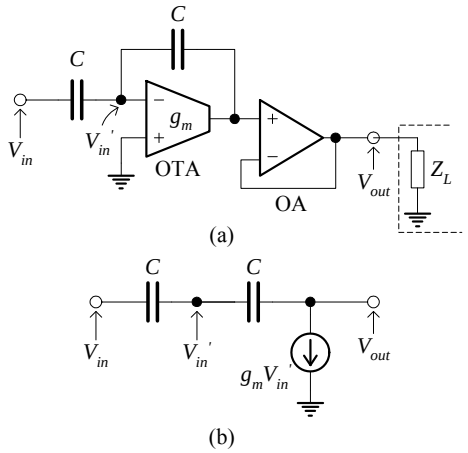



Figure 2. All-pass filter: electrical scheme (a) and model (b)

The circuit, sketched in Fig. 2(b), is modeled by the following transfer function:

$$H(s)=\frac{V_{out}}{V_{in}}=\frac{s-\frac{g_m}{C}}{s+\frac{g_m}{C}} \tag{1}$$

Its amplitude characteristic is given by:

$$\left|H(\omega)\right|=1, \tag{2}$$

whereas the phase characteristic can be written as:

$$\theta(\omega)=-2\arctan\left(\frac{\omega C}{g_m}\right). \tag{3}$$

Both, the amplitude and the phase characteristics are defined in the term of admittance $\omega C$ and amplifier transconductance $g_m$. We have two design choices at disposal, herein. Namely, filter phase characteristics can be tuned either by varying capacitance of capacitor $C$ or OTA transconductance $g_m$. From the aspect of CMOS technology, the better and the efficient solution is that one based on transconductance $g_m$ control. In this paper, the latter mentioned approach is used for all-pass filter design.

The structure of OTA, used for implementation of the all-pass filter, is depicted in Fig. 3. It has a form of single stage telescopic architecture [13], [14]. The input differential pair, consisting of transistors $M_1$ and $M_2$, injects current signals into transistors $M_5$ and $M_6$, which operate as common gate amplifiers. Cascode current mirrors, composed of transistors $M_7$, $M_8$ and $M_9$, $M_{10}$, provide differential (symmetrical) to single ended output conversion. In order to create telescopic composition, transistors are placed one on the top of the other. The output resistance is high due to serial connection of two cascode configurations [13].

Notice that polarization of transistor $M_3$ is not standard. Namely, the gate of transistor $M_3$ is directly connected to a bias control voltage $V_{bias}$. The voltage $V_{bias}$ defines a sink current $I_{SS}$ of the differential stage (transistors $M_1$, $M_2$). The transconductance $g_{md}$ of the differential stage is given by:

$$g_{md}=\sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_{M_1,M_2} I_{ss}}\,, \tag{4}$$

where $I_{SS}$ is:

$$I_{ss}=\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{M_3}\left(V_{bias}-V_{Th}\right)^2. \tag{5}$$

For more details related to (4) and (5), someone can refer to [13]. By implementing OTA with voltage-controlled transconductance, contrary to the traditional approach (OTA with constant $g_m$), provide us to realize a voltage-controlled $g_m$–$C$ all-pass filter [8]-[12].

OTA is implemented in IHP 0.25 μm SiGe BiCMOS technology, with the supply voltage $V_{dd}$ =3 V [18]. OTA characteristics depend on gate bias voltage of transistor $M_3$. In the middle of a regulation range, with $V_{bias}$ = 0.7 V, OTA has the first pole at $f_p$= 1.1MHz, gain-bandwidth product GBW=600 MHz, open loop gain $A_0$=62.5 dB, and output resistance $R_{out}$ = 2.4 MΩ.

OA, shown in Fig. 3 (b), is designed as the simple single stage differential amplifier [13], realized by transistors $M_1$ and $M_2$, and current mirror ($M_4$ and $M_5$) intended for differential to single ended output signal conversion. OA operates as non-inverting amplifier with unity gain and 3 GHz cutoff frequency. Its influence on amplitude and phase characteristics of the all-pass filter is negligible.

Phase characteristics of the first-order all-pass filter (see Fig. 2), obtained by Spice simulation, are presented in Fig. 4(a). The filter is realized with OTA given in Fig. 3(a) and capacitor $C$ = 1 pF. Simulations have been carried out for different values of control voltage $V_{bias}$ (0.4V up to 0.85V), in the frequency range from 10 kHz up to 1 GHz. By analyzing the obtained results, we can conclude that phase shifts of all characteristics start from –180° and end with –360°. When $V_{bias}$ varies from 0.4V to 0.85V, mid-points

move towards higher frequencies on all curves (the phase shift –270°). For example, the phase shift of –270° is at frequency of 100 kHz for $V_{bias}$= 0.4V, whereas for $V_{bias}$= 0.85V, it is at frequency of 200 MHz, what corresponds to three decades regulation range.

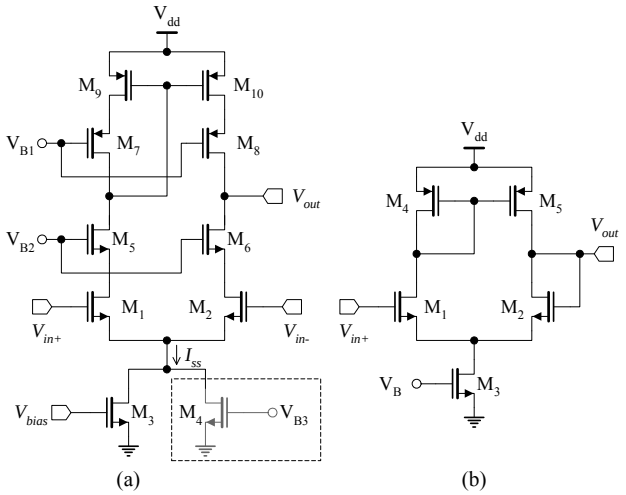



Figure 3. Schematics of OTA (a) and OA (b)

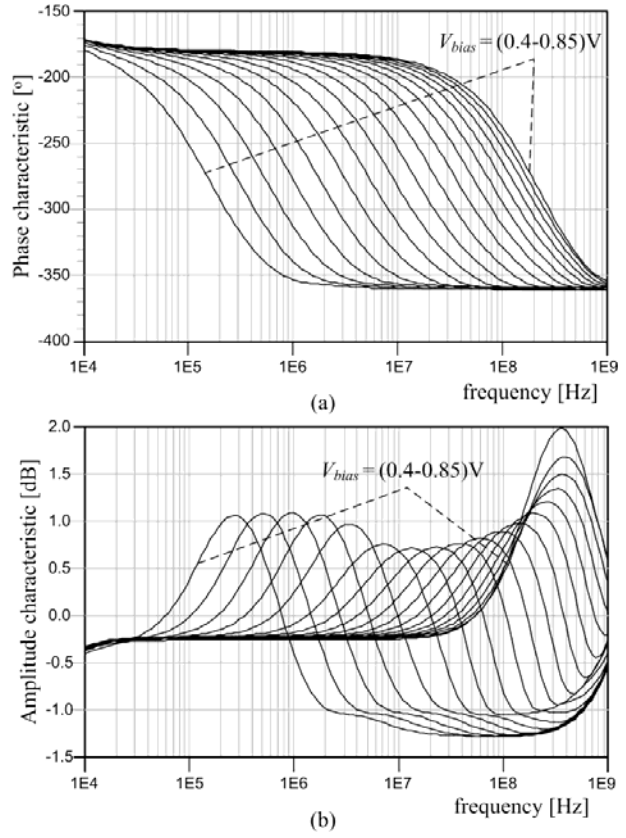



Figure 4. Phase (a) and amplitude (b) characteristics of $g_m$–$C$ all-pass filter

Theoretically, the amplitude characteristic of a voltage-controlled all-pass filter should be completely flat and does not depend on frequency and bias voltage. Because of discrepancy of capacitance $C$ and OTA imperfections, filter amplitude response deviates from the ideal one. Amplitude characteristics are obtained by using Spice simulations in the frequency range between 10 kHz and 1 GHz and for different $V_{bias}$ values, from 0.4 V up to 0.85 V. As can be seen from the obtained results, amplitude characteristics vary more than 2 dB, in the frequency range of interest. However, it is expected that deviations of amplitude characteristics will be less than 1 dB when the preferred operating point of filter is set for the phase shift of -270 °.

The transient time-responses of all-pass filter are presented in Fig. 5. The responses are obtained by simulation for different values of bias voltage $V_{bias}$ (0.4 V to 0.85V), and the input signal of 50 MHz frequency. As can be seen from Fig. 5 for wide phase-shift variation (from -180$^0$ up to -360$^0$) amplitude of the output signal is almost constant ±0.9 dB. The obtained results are expected having in mind all-pass filter characteristics (Fig. 4(b)).

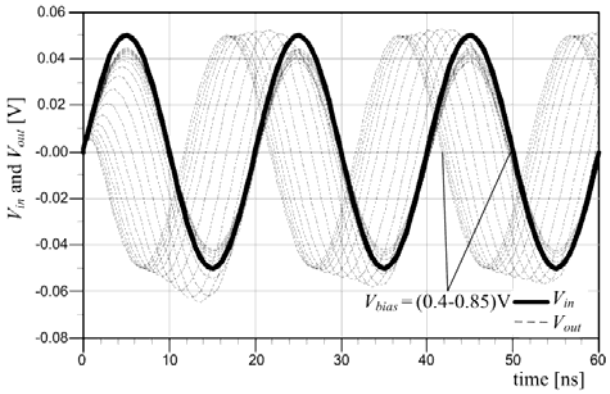



Figure 5. Transient time-response of $g_m$–$C$ all-pass filter

## III. PHASE-SYNCHRONIZER

When several voltage–controlled $g_m$–$C$ all-pass filters are connected in a chain, we obtain a building block for which the amplitude response $V_{out}$ / $V_{in}$ is constant, while the phase of $V_{out}$ can be adjusted in a wide range by implementing a phase loop control method. The basic idea of the phase control is similar to one we meet in DLL circuits [2]-[4], with one exception: instead of pulse delay control as it is in DLL circuits, we control here the phase of analog output signal [17]. The block diagram of the proposed circuit is given in Fig. 6.

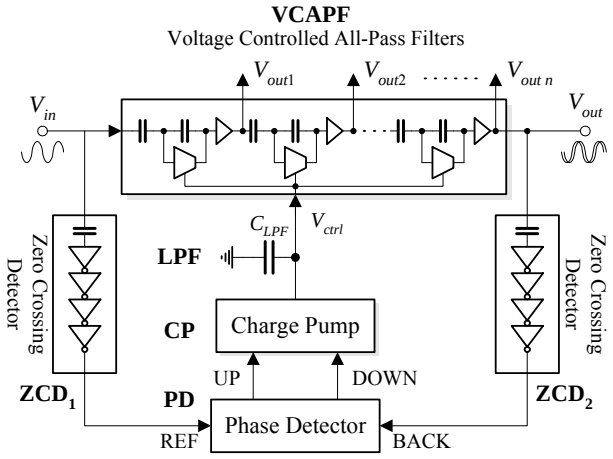



Figure 6. Block diagram of phase-synchronizer

In order to evaluate the phase shift between $V_{out}$ and $V_{in}$, it is necessary to amplify signals $V_{out}$ and $V_{in}$ first, and after that to shape them to rectangular form. This is achieved by using a zero crossing detector (ZCD). Phase comparison of input $V_{in}$ and output $V_{out}$ signals is performed by a phase detector (PD), which generates UP and DOWN signals. DOWN signal is on when the $V_{out}$ phase leads in respect to the $V_{in}$ phase, while in the opposite, UP signal is active. Time durations of UP and DOWN signals are proportional to the phase shift. UP and DOWN signals control operation

of a charge pump (CP). CP charges and discharges the load capacitor $C_{LPF}$ providing $V_{ctrl}$ that is used as control voltage for the all–pass filter chain. In stable-state the phase shift between $V_{out}$ and $V_{in}$ signals is 360°.

ZCD is implemented by the circuit presented in Fig. 7. It is composed of four CMOS inverter stages, denoted by $A_1$ to $A_4$. The first stage, $A_1$, acts as a linear amplifier. Since its input is capacitive coupled with the analog signal obtained from the VCAPF, it eliminates the DC offset. The other three stages, $A_2$, $A_3$ and $A_4$, operate as digital inverter stages.

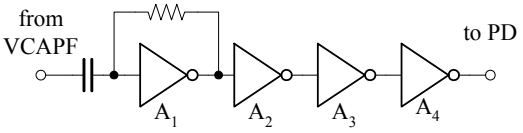
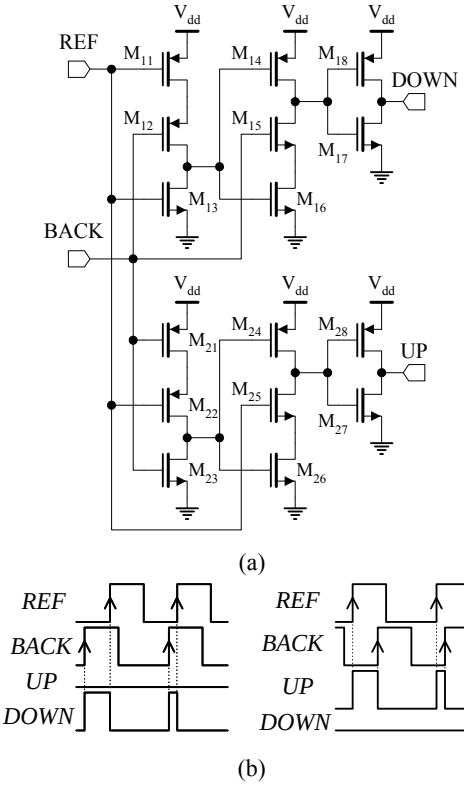



Figure 7. Zero crossing detector




(a)




(b)

Figure 8. Schematic of phase detector (a) and signals waveforms (b)

PD, shown in Fig. 8(a), measures the phase difference between the reference signal REF (the output of $ZCD_1$) and the output signal BACK (the output of $ZCD_2$), and generates output signal whose duration is proportional to the detected phase error. Its hardware structure is adopted from [3]. The main advantages of PD are: *i*) simple hardware structure, *ii*) high-speed of operation and *iii*) small dead zone [3], [4]. PD output signals, UP and DOWN, are used to control the operation of CP circuit. PD is sensitive to rising pulse edges.

The PD operation principle is depicted in Fig. 8(b). As we mentioned earlier, the widths of UP and DOWN signals are proportional to the phase difference between REF and BACK signals. Waveforms on the left side of Fig. 8(b) correspond to the case when BACK signal leads in respect to REF signal. Diagrams on the right side are valid when REF signal leads in respect to BACK signal.

The structure of CP capacitive loaded with $C_{LPF}$ as loop filter is presented in Fig. 9. Transistors $M_1$ and $M_4$ act as switching elements driven by UP and DOWN pulses, whereas transistors $M_2$ and $M_3$ are employed as current sink and source, respectively. CP charges or discharges the phase loop filter capacitor $C_{LPF}$. The control voltage $V_{ctrl}$ drives VCAPF.

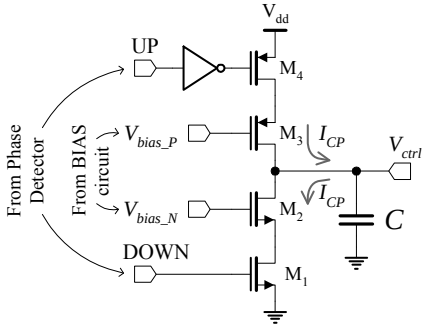



Figure 9. Charge pump with phase loop filter

CP acts as an integrator and, therefore, $V_{ctrl}$ can be written as:

$$V_{ctrl} = -k_{cp} \int_{-\infty}^{t} \theta \mathrm{d}\tau \,, \tag{6}$$

where $k_{cp}$ is a CP gain. The CP gain depends on $I_{CP}$ (constant current of a charge pump – see Fig. 9) and the capacitor $C_{LPF}$. The CP current $I_{CP}$ used for charging or discharging $C_{LPF}$, is set to small value. This allows direct on-chip implementation of the phase loop capacitor $C_{LPF}$.

The bias circuit is intended to provide correct CP operation. This block generates two bias voltages, $V_{bias\_P}$ and $V_{bias\_N}$. More design details, which relate to the bias circuit, are given in [4]. The control voltages, $V_{bias\_P}$ and $V_{bias\_N}$, define charging and discharging currents of $C_{LPF}$. In our case, $I_{CP}$ =75μA and $C_{LPF}$ = 10pF.

In stable-state, the total phase-shift involved by VCAPF should be –360°. To achieve this goal, each all-pass filter stage involves a phase shift of –360°/*n*, where *n* is the number of filter stages in the chain. The phase difference between $V_{outi}$ and $V_{outi\text{-}1}$, $i$=1,...,$n$, is equal to 360°/*n*. In this manner, multiphase signals at the VCAPF's outputs are obtained. In general, multi-phase outputs can be used in numerous applications including modulators, demodulators, frequency converters etc.

Each filter can introduce any phase shift in the range from –180° up to –360° (see Fig. 4(a)). This means that stable operation can be achieved when each filter stage involve phase shift of –180° and *n* is an even number, or when the all filter stages insert phase shift of –360° for arbitrary *n*. This brings to the trivial solution, discussed hereafter.

The first case, when *n* is even, is not possible. This situation only happens at very low frequencies that are outside of the circuit operating range (<100 kHz). However, the second case is possible especially when the control voltage $V_{ctrl}$ has small value (typical for the initial time instant). According to Fig. 4(a), for minimal $V_{ctrl}$ all filter stage involve maximum phase shift ($-360^0$). The problem can be solved by increasing the transconductance, i.e. by increasing the operating current of OTA. For that purpose, the transistor $M_4$ is added into OTA (Fig. 3(a)), acting as a constant current source. By involving such modification the

filter stage can inserts a phase shift of –360° at very high frequencies (>200 MHz), which are outside of the VCAPF operating range. The drawback of this solution is narrower frequency operating range of the phase-synchronizer.

## IV. Stability Analysis

The phase of *n*-stage voltage-controlled all-pass filter chain is defined by:

$$\theta_n = -2 \cdot n \cdot \arctan\left(\frac{\omega C}{g_m}\right), \tag{7}$$

with $g_m$ determined as:

$$g_m = g_{m_d} + g_{m_c}, \tag{8}$$

where $g_{m_c} = \text{const.}$ and:

$$g_{md} = k_{m_d}\left(V_{ctrl} - V_{th}\right), \tag{9}$$

with $V_{ctrl}$ corresponding to $V_{bias}$ in (5), and:

$$k_{m_d} = \mu C_{ox}\sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_{M_1}\left(\frac{W}{L}\right)_{M_2,M_3}}. \tag{10}$$

The phase shift of output signal for *i*-th stage is given by

$$\theta_i = -2 \cdot i \cdot \arctan\left(\frac{\omega C}{g_m}\right), \qquad 1 \le i \le n. \tag{11}$$

Let note that multi-phase signals, $V_{out1},...,V_{outn}$ are generated at the outputs of each all-pass filter in the chain.

The stability issue of the proposed solution is discussed by proving the following theorem.

Theorem1: The phase loop of the all-pass filter chain, defined by (7), (8) and (9), with the control (6), where $\theta=\theta_n$, is globally asymptotically stable, implying that $\theta_n$ tends to zero ($\theta_n \to 0$) for any initial non-zero value of the phase shift.

*Proof:* The phase loop dynamics is directly obtained by time-differentiation of (7):

$$\frac{\mathrm{d}\theta_n}{\mathrm{d}t} = -\frac{2nk_{cp}k_{m_d}\omega C}{\left(k_{m_d}\left(V_{ctrl} - V_{th}\right) + g_{m_c}\right)^2 + \left(\omega C\right)^2}\theta_n, \tag{12}$$

taking into account (6), (8) and (9).

In order to prove that the phase dynamics (12) is stable, we will use the Lyapunov stability theorem [15]. The Lyapunov function candidate *V* is chosen to be:

$$V = \frac{1}{2}\theta_n^2. \tag{13}$$

As we can see, it is positive definite function $V > 0$ for $\forall \theta_n \neq 0$, $V=0$ for $\theta_n = 0$ and $V \to \infty$ when $\theta_n \to \infty$. Since its time–derivative:

$$\frac{\mathrm{d}V}{\mathrm{d}t} = \theta_n\frac{\mathrm{d}\theta_n}{\mathrm{d}t} = -\frac{2nk_{cp}k_{m_d}\omega C}{\left(k_{m_d}\left(V_{ctrl} - V_{th}\right) + g_{m_c}\right)^2 + \left(\omega C\right)^2}\theta_n^2 < 0 \tag{14}$$

is negative definite function for $\forall \theta_n \neq 0$, according to the Lyapunov stability theorem [15], one can conclude that the equilibrium point of (12) $\theta_n = 0$ and, consequently, the overall system are globally asymptotically stable, i.e. the phase $\theta_n$ tends to zero asymptotically from any initial non-zero value.

## V. Simulation Results

The proposed approach, which relates to design of $g_m$–*C* all–pass filter chain with phase loop control, is verified by Spice simulation. The IHP design kit for 0.25 μm SiGe BiCMOS technology was utilized [18]. The supply voltage $V_{dd}$ is chosen to be 3V.

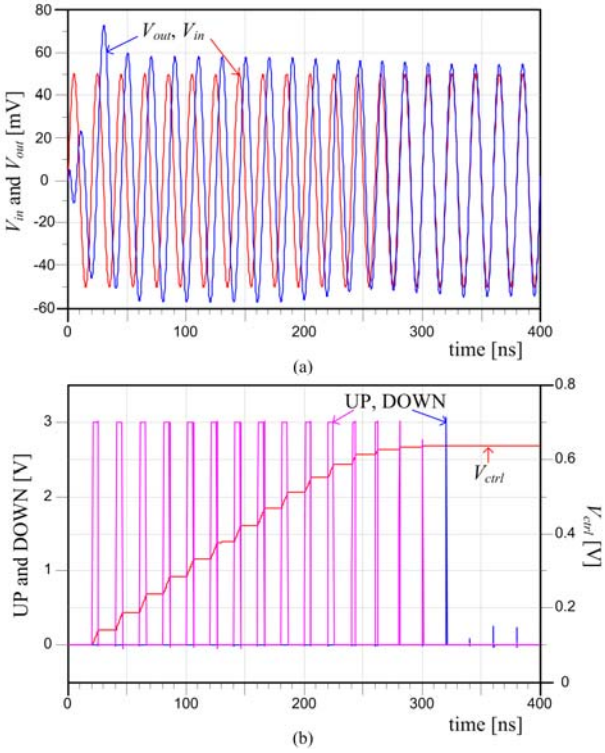



Figure 10. Spice simulation results of the proposed circuit

Fig. 10 depicts time response of the phase-synchronizer. Waveforms of input signal $V_{in}$ and output $V_{out4}$ for four stage all-pass filter chain ($n$ = 4) are presented in Fig. 10(a). The frequency of input signal is $f$ = 50 MHz. The waveforms of UP and DOWN signals, obtained at the outputs of PD, as well as $V_{ctrl}$, are given in Fig. 10(b). The steady-state state is reached, i.e. the phase loop is locked, at the moment when: *i*) the phases of signals $V_{in}$ and $V_{out}$ are equal, *ii*) UP and DOWN signals disappear, and *iii*) the control voltage $V_{ctrl}$ has constant value. The settling time is approximately 300 ns.

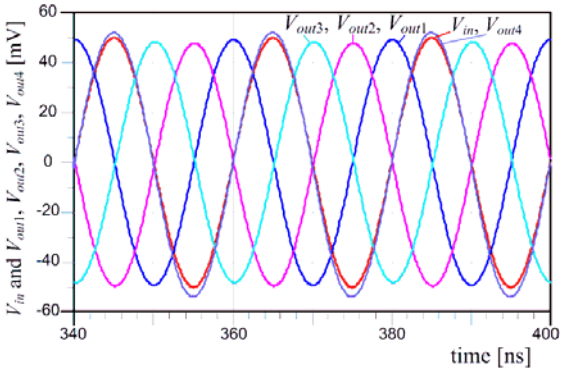



Fig.11. Waveforms of input signal and stage output signals in all-pass filter chain

The steady-state waveforms of VCAPF output signals are given in Fig. 11. As it can be seen, the phase shift between input $V_{in}$ and output $V_{out4}$ signals is 360°. Consequently, the phase shift between the adjacent stages in the filter chain is 90°.

## VI. PHASE-SYNCHRONIZER APPLICATION EXAMPLES

The phase-synchronizer is commonly used as building block in many communication, RF circuits and systems. The most often application relates to phase-shifter. Usually, the phase-shifter is implemented as a block, which provides fixed phase shift $\alpha$, both at given frequency, or in a narrowband. In this case, the phase-shifter has unity gain, and therefore does not influence on signal amplitude. Fig. 12(a) shows how a phase-synchronizer can be used as a phase-shifter. In this design the number $n$ of all-pass filters in a chain is selected to fulfill a condition $\alpha = 360^{o} / n$.

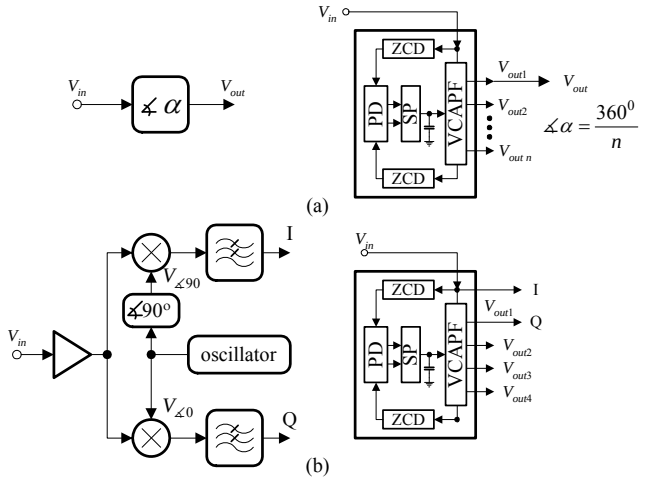



Fig. 12. (a) Phase shifter, (b) quadrature carrier multiplexer

In many modulation/demodulation schemes, the carrier signal should contain both, in-phase and quadrature phase components [19]. The input signal, $V_{in}$, is multiplied with in-phase signal, $V_{\measuredangle 0}$, and with quadrature signal, $V_{\measuredangle 90}$, of the local oscillator. The baseband output signals, I and Q, (see Fig. 12(b)) are in-phase and quadrature in respect to the input signal. As is sketched in Fig 12(b), the phase-synchronizer acts as a quadrature carrier multiplexer. Its chain VCAPF consists of four all-pass filters.

## VII. CONCLUSION

The paper deals with phase-synchronizer based on voltage-controlled $g_m$–$C$ all-pass filters chain. Different kinds of issues in regard to phase-synchronizer were presented in this paper. As a first, the crucial property of the proposed approach relates to phase correction of analog input signal achieved by the voltage-controlled all-pass filters chain. The control is realized using phase loop. The second property deals with two novelties. The first one concentrates on design of the voltage-controlled all-pass filter. The continuous-time $g_m$–$C$ filter is used since it is suitable for on-chip implementation, contains small number of lumped elements, and operational transconductance amplifier whose transconductance $g_m$ can be easily tuned. The second novelty concentrates on analog signal preprocessing of the phase detector input signal. Since analog signals are sinusoidal, with variable amplitude and phase, they have to be shaped first by using zero crossing detectors. Zero crossing detector transforms analog input signals into pulse trains, and drives the digital phase detector. Finally, the stability of all-pass filter chain with phase loop control is proved by the Lyapunov stability theorem. The proposed circuit can be used as building block in modulators and demodulators, frequency synthesizers, clock generation and recovery, filtering, suppression of symmetrical signals in up/down frequency converter, etc. The IHP 0.25 μm SiGe BiCMOS technology was used in design and verification of the all–pass filter chain with phase loop control. According to the simulation results, it is possible to obtain phase regulation in the wide frequency range, starting from 100 kHz up to 200 MHz. The described phase-synchronizer is intended to be a building block (cell) of common RF library.

## REFERENCES

[1] David Boerstler, "A Low-Jitter PLL Clock Generator for Microprocessors with Lock Range of 340–612 MHz," *IEEE J. of Solid-State Circuits*, Vol. 34, No. 4, pp. 513-519, April 1999.

[2] John Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, November 1996.

[3] Y. Moon, et al., "An All-Analog Multiphase DLL Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 377-384, March 2000.

[4] M. Stojčev and G. Jovanović, "Clock aligner based on delay locked loop with double edge synchronization," *Microelectronics Reliability*, vol. 48, no. 1, pp. 158–166, January 2008.

[5] J. Yuan, et al., "High-Speed CMOS Circuit Technique," *IEEE J. Solid-State Circuits*, vol. 24, no.1, pp. 62-70, February 1989.

[6] B.P. Das, N. Watson, Liu Yonghe, "Wide Tunable All Pass Filter Using OTA as Active Component," *International Conference on Signals and Electronic Systems (ICSES)*, 2010, pp. 379-382.

[7] Chun-Ming Chang, B.M. Al-Hashimi, "Analytical synthesis of voltage mode OTA-C all-pass filters for high frequency operation, Circuits and Systems," *Proceedings of the International Symposium on ISCAS '03*, May 2003, pp. 461-464.

[8] Radu Gabriel Bozomitu, Neculai Cojan, "A VLSI Implementation of a New Low Voltage 5th Order Differential Gm-C Low-Pass Filter with Auto-Tuning Loop in CMOS Technology," *Advances in Electrical and Computer Engineering*, vol. 11, no. 1, pp. 23-30, 2011.

[9] T. Sanchez Rodriguez, et al., "A CMOS Linear Tunable Transconductor For Continuous-Time Tunable Gm-C Filters," *Circuits and Systems, IEEE International Symposium on ISCAS*, 2008, pp. 912-915.

[10] M. Pedro, et al., "A low-pass filter with automatic frequency tuning for a bluetooth receiver," *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2010, pp. 462-465.

[11] Zhong Yuan Chang, D. Haspeslagh, and J. Verfaillie, "A Highly Linear CMOS Gm-C Bandpass Filter with On-Chip Frequency Tuning," *IEEE J. of Solid-State Circuits*, vol. 32, no. 3, pp.388-397, March 1997.

[12] C. David, et al., "A Gm–C Low-pass Filter for Zero-IF Mobile Applications With a Very Wide Tuning Range," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1443-1450, July 2005.

[13] Franco Maloberi, *Analog Design for CMOS VLSI Systems,* Kluwer Academic Publisher, Boston, 2001.

[14] Mrinal Das, "Improved Design Criteria of Gain-Boosted CMOS OTA With High-Speed Optimizations," *IEEE Transactions on Circuits and Systems II*: vol. 49, no. 3, pp. 204-207, March 2002.

[15] H. K. Khalil, *Nonlinear Systems*, Prentice Hall, Inc., USA, 1996.

[16] K. Bult and H. Wallinga, "A CMOS Analog Continuous-Time Delay Line with Adaptive Delay-Time Control," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 759-766, June 1988.

[17] Goran Jovanović, Mile Stojčev, "A Delay Locked Loop for Analog Signal," *in Proc. of 9-th International Conference TELSIKS*, vol. 1, Niš, Serbia, October 2009, pp. 233-236.

[18] IHP-Microelectronics, SiGe:C BiCMOS Technologies for MPW & Prototyping, http://www.ihp-microelectronics.com/16.0.html.

[19] Pui-In Mak, Seng-Pan U, Rui Paulo Martines , *Analog-Baseband Architectures and Circuits for Multistandard and Low-Voltage Wireless Transceivers*, Springer, Netherlands, 2007.