Static Frequency Converter with RNSIC Converter and Double Branch Inverter for Supplying Three-Phase Asynchronous Motors

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Abstract — **The paper presents the design and analysis of a three-phase static converter, composed of a Rectifier with Near Sinusoidal Input Currents (RNSIC), which ensures the DC bus voltage level for a three phase Incomplete Bridge Inverter (IBI), used to drive an asynchronous motor. The proposed circuit has a low input current harmonic content, can ensure the load overcurrent protection and has a better reliability. The converter can be designed to provide any required output maximum power under a desired DC link bus voltage.**

Index Terms — **asynchronous motors, converter, DC bus voltage, RNSIC (Rectifier with Near Sinusoidal Input Currents), three - phase Incomplete Bridge Inverter (IBI)**

I. INTRODUCTION

One of the most important tasks of Power Electronics converters is to drive asynchronous motors with adjustable speed. The reference converter used for this application is presented in Figure 1, and it basically contains a three phase bridge diode rectifier, followed by a three phase full bridge converter [1].

In the last period, considerable efforts were made to reduce the number of harmonics injected into the system. In order to solve this issue, different approaches were made, starting from the insertion of efficient filtering blocks, connected in parallel to the circuit, and ending to the design of high performance rectifiers, which have an unitary power factor and inject a low content of harmonics into the system. The use of filtering blocks can achieve high performances, provided active filters are used. This fact implies greater initial cost and inability of constructing large – rated current sources with a rapid current response [2 – 7].

A good alternative is the pulse width modulation voltage source rectifier (PWM – VSR) depicted in Figure 2, which ensures an almost sinusoidal input current, controllable input factor and current regeneration capacity**.** PWM – VSR can be used in high performance adjustable speed driven applications that demand an enhanced control for the DC link voltage and present operating cycles with continual transitions between motoring and regeneration. The cost needed for this rectifier is at least double in comparison to the common rectifiers. There are many applications where the asynchronous motors are not working in the regeneration state and the required dynamical response is average.

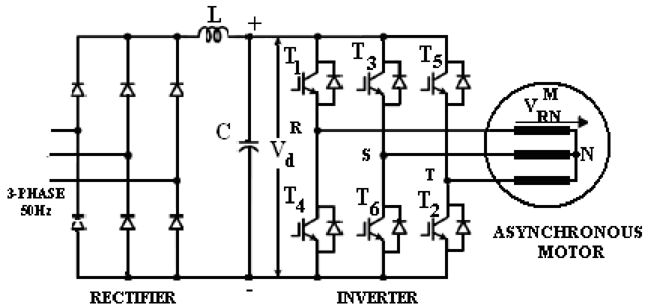

Figure 1.Basic static converter circuit for an asynchronous motor drive

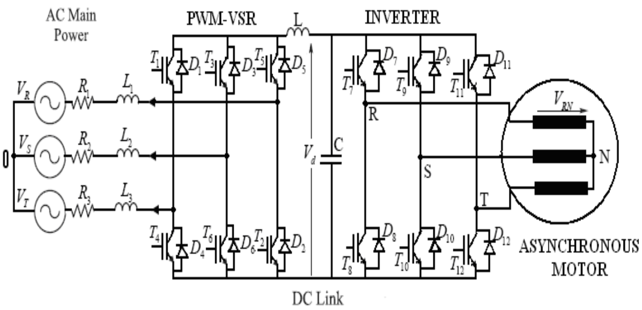

Figure 2.Static converter with PWM – VSR

The main demands for these types of situations are low cost, high reliability and low current harmonic injection. In the last period, several phase rectifiers were proposed.

A very attractive one is the three phase RNSIC converter [2], [8], [9] which is able to ensure both a lower harmonic current injection into the AC main and a higher output DC voltage, due to it's L – C AC input filter. The major drawback of this rectifier is the variation of the output voltage, when the load experiences large variations. Thus, the suitable applications for this circuit are limited to the ones that have loads which either absorb power and are insensitive to the DC voltage variation, or are able to readjust the DC voltage bus (battery charging). On the other hand, the three phase IBIs are cheaper than the three phase full bridge ones, but the use of these inverters is restricted due to their lower output voltage. The RNSIC (high output voltage amplitude) and the IBI (low output voltage amplitude) can be combined in order to obtain both the desired voltage amplitude for an asynchronous motor and ensure a low harmonic injection into the AC main.

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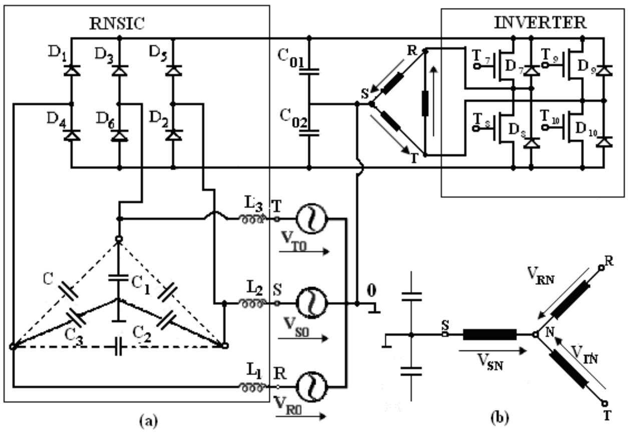

Figure 3.Proposed static frequency converter composed of a RNSIC converter and an Incomplete Bridge Inverter for supplying three - phase asynchronous motors

II. CIRCUIT DESCRIPTION AND DESIGN

The proposed circuit is depicted in Figure 3a. The RNSIC converter contains the diode bridge $D_1 - D_6$, the inductances $L_1 = L_2 = L_3 = L$ and three equal star connected capacitors $C_1 = C_2 = C_3 = C$. The three-phase IBI is composed of the transistors $T_7 - T_{10}$, the diodes $D_7 - D_{10}$ and the equally large capacitors C_{01} and C_{02} ($C_{01} = C_{02} = C_0$). The capacitive voltage divider leg of the IBI also serves as a DC – link to the RNSIC output voltage (V_D). The motor's stator winding is triangle connected [9]. In this situation the voltage amplitude across one winding (for instance U_{RS} in Figure 3a) is equal to:

$$U_{RS\max} = \frac{V_D}{2} \tag{1}$$

In case a star stator winding connection is used (Figure 3b), then the voltage amplitude across the winding is equal (for example V_{SN}) to V_D /3 (T_8 – ON; T_{10} – ON; T_7 – OFF; T_9 – OFF).

The triangle connection is by far a better choice, in case the IBI is used.

The standard rectifier depicted in figure 1 ensures a maximum DC bus voltage level equal to $\sqrt{3}\,U_M$= 538V, where U_M is the phase voltage amplitude equal to 311V.

In case the three-phase Full Bridge Inverter (FBI) uses the sinusoidal PWM modulation, the phase voltage amplitude (for instance V_{R0}) is:

$$V_{0MAX} = \frac{\sqrt{3}U_M}{2} \approx 269V \tag{2}$$

In order to provide the nominal supply conditions for an asynchronous motor (50Hz and 311V for each phase), the inverter shown in figure 1 is usually driven through overmodulation techniques. This approach enables the increase of the phase voltage on each phase to a level close to the nominal value (U_M = 311V). The main drawback of overmodulation control refers to the decrease of the efficiency, due to the increase of the distortion coefficient of the inverter's output voltage.

If a square wave modulation is used for the circuit plotted in Figure 1, the phase to load the neutral voltage (for example V_{RN} in Figure 1) has a maximum value of:

$$V_{0MAX} = \frac{2}{3}\sqrt{3}U_M \approx 360V \tag{3}$$

Not only the overmodulation method suffers from these types of disadvantages, but also the square wave modulation experiences problems regarding the output voltage harmonics increase.

The DC bus voltage of the circuit illustrated in Figure 3 can be improved, provided a RNSIC is used. In this way, only sinusoidal modulation is required for obtaining an output inverter voltage amplitude equal or greater to that of the FBI with square wave modulation (equation 3).

Initially, it is necessary to find out the DC – link voltage value for which the asynchronous motor connected to the output of the IBI, receives the same maximum voltage as it would receive when connected to the output of the FBI.

In order to determine the necessary value of the RNSIC output voltage V_D, equation (1) is combined with equation (3).

From equations (1) and (2), the necessary RNSIC output DC – link voltage is expressed as:

$$V_D = \frac{4}{3}\cdot\sqrt{3}\cdot U_M \approx 720V \tag{4}$$

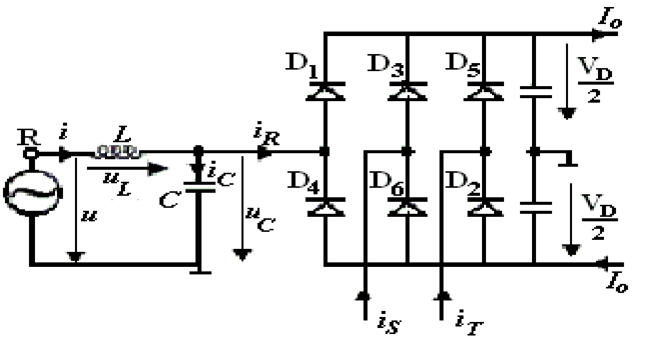

Figure 4.RNSIC equivalent circuit depicted for one phase

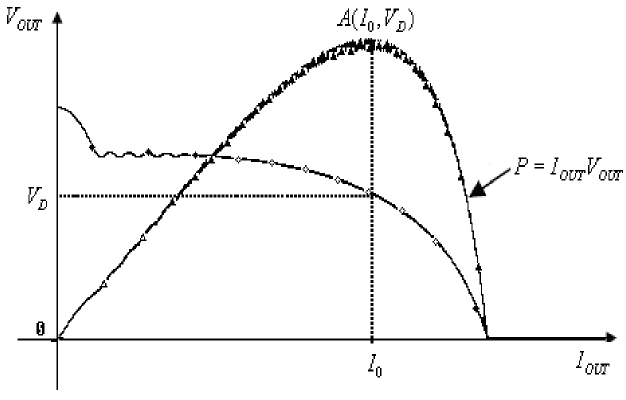

Figure 5.RNSIC output electrical parameters variation

The phase supply electrical behavior can be analyzed according to the equivalent circuit depicted in Figure 4 and the behaviors of the electrical parameters from Figure 4 are plotted in Figure 5.

In order to satisfy equation (4), the condition (5) has to be fulfilled:

$$n^2 = \frac{\omega_0^2}{\omega^2} < \frac{1}{1-2\frac{U_M}{V_D}} \approx 7.4 \qquad (5)$$

where $\omega_0^2 = 1/LC$.

The typical variation of the output voltage and power of a RNSIC converter against the output current are represented in Figure 5. From this, it can be deducted that the output power trace has a maximum value for point $A(I_0, V_D)$. It is essential to observe that when the RNSIC operates in point A, the supply current and voltage are in phase ($\varphi = 0$).

For a value lower than I_0 of the output current (point A), the RNSIC has a capacitive behavior ($\varphi < 0$), whereas for a higher output current, the RNSIC has an inductive behavior ($\varphi > 0$). The optimal choice is to design the RNSIC circuit to generate a maximum output power equal to the maximum nominal value of the asynchronous motor. The maximum output voltage is reached when the output current is $I_{out} = 0$ and can be described by:

$$V_{CMAX} = 2\frac{n^2}{n^2-1}U_M \qquad (6)$$

When the current absorbed by the load is less than I_0, the output characteristic for the RNSIC is higher, but it must be much less than the breakdown voltage of an asynchronous motor (which is higher than 1.5kV). This working regime appears when the motor is turned off. In applications with no critical speed variations and with no inertial load (proper for this type of circuit), the motor voltage stress can be easily controlled.

Furthermore, another advantage of the RNSIC is the limitation of the output power that takes place when the output current is higher than the nominal value I_0. That prevents the motor from heating and breaking down when an unwanted overcurrent appears.

If the phase current i(t) is considered as reference, the value of both phase current and voltage (Figure 4), will be:

$$\begin{aligned} i(t) &= I_M \sin(\omega t) \\ u(t) &= U_M \sin(\omega t + \varphi) \end{aligned} \qquad (7)$$

For the interval $\omega t \in [0, \pi]$, two stages can be described.

The first stage is for $\omega t \in [0, \omega t_1]$ when the diodes D_1 and D_4 are OFF and the capacitor is charged from $-V_D/2$ up to $V_D/2$ (Figure 6).

The circuit behavior is described by:

$$u(t) = u_L(t) + u_C(t) \qquad (8)$$

With the solution:

$$u_C(t) = \left[\frac{n}{n^2-1}U_M \cos\varphi\right]\sin(n\omega t) - \left[E + \frac{n^2}{n^2-1}U_M \sin\varphi\right] \cos(n\omega t) + \frac{n^2}{n^2-1}U_M \sin(\omega t + \varphi) \qquad (9)$$

$$i(t) = C\frac{du_C(t)}{dt}$$

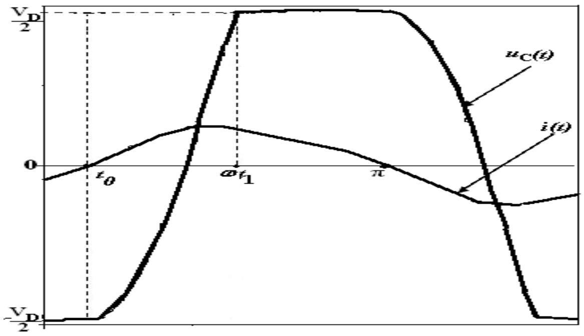

Figure 6.Phase input current and voltage across capacitor C

For this stage, the circuit behavior is capacitive (n>1) and the current i_R is zero. During this stage the electrical charge transferred from the main to the capacitor C is Q_{S1}. This stage lasts until time t_1, when the following conditions are fulfilled:

$$\begin{aligned} Q_{S1} &= CV_D \\ u_C(t_1) &= \frac{V_D}{2} \\ i(t_1) &= I_1 \end{aligned} \qquad (10)$$

The second stage is for $\omega t \in [\omega t_1, \pi]$. For this stage, i_C is zero and the input phase current is transferred to the output capacitor $C_{01} = C_0$. The current through diode D_1 is found out from:

$$u(t) = \frac{V_D}{2} + u_L(t) = \frac{V_D}{2} + L\frac{di}{dt}; t \in \left[t_1, \frac{\pi}{\omega}\right] \qquad (11)$$

With the solution:

$$i(t) = I_1 + \frac{U_M}{\omega L}\left[\cos(\omega t_1 + \varphi) - \cos(\omega t + \varphi)\right] + \frac{E}{\omega L}(\omega t_1 - \omega t) \qquad (12)$$

During this stage the electrical charge transfer from the main to the inductance L and the diode D_1 is Q_{S2}. This charge is 1/6 of the total charge which feeds the IBI during a supply input voltage period. Furthermore, if the phase current is zero at point π/ω, then the circuit is completely described with the help of two more equations:

$$\begin{aligned} Q_{S2} &= \frac{\pi}{3\omega}I_0 = \int_{t_1}^{\pi/\omega} i(t)dt \\ i\left(\frac{\pi}{\omega}\right) &= 0 \end{aligned} \qquad (13)$$

The latter from the equations (13), means that during the second stage, one third of the electrical charge which is transferred to the output capacitor C_{01} is generated through diode D_1.

For optimal design, I_0 and V_D are supposed to be given, and (9), (10), (12) and (13) are evaluated on condition $\varphi = 0$ (the input phase current and voltage are in phase). Furthermore, the 'n' parameter has to respect the following requirement:

$$1.5 \le n \le 2 \tag{14}$$

The lower the value of 'n', the lower the harmonic content for the phase current that will be generated is. The selection of parameter 'n' must be done according to equation (6). The maximum RNSIC output voltage has to be less than 75 % of the motor's breakdown voltage.

II.1 A PRACTICALLY EFFICIENT DESIGN

In order to obtain the necessary values for L and C, given the output values of the RNSIC voltage (V_D) and current (I_0), first the 'n' – parameter has to be selected according to condition (14). The second step is the computation of either L or C from the empirical equation (15) using (16):

$$Q_{S1}\frac{1}{\omega C} = \omega L\left(Q_{S1} + Q_{S2}\right) \tag{15}$$

$$LC = \omega^2 n^2 \tag{16}$$

where Q_{S1} and Q_{S2} represent the electrical charges transferred through one half phase during the first and second stages, respectively.

III. INVERTER CONTROL STRATEGY

In Figures 3a and 7, the IBI output voltages are u_{RO} and u_{TO}, whereas the three phase stator voltages are u_{RS} , u_{ST} and u_{TR}. The voltage u_{RS} is in phase with u_{RO}, but the voltage u_{ST} (which has a 120° phase difference against u_{RS}) has a 180° phase difference as referred to u_{TO}. On conclusion the modulation signals u_a and u_b (Figure 9a) have to have a 60° phase difference in order to provide a proper PWM sinusoidal control of the IBI [10].

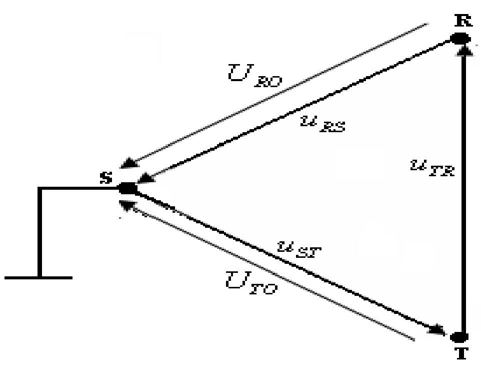

Figure 7.Vectorial representation of the stator voltage according to Figure 3a

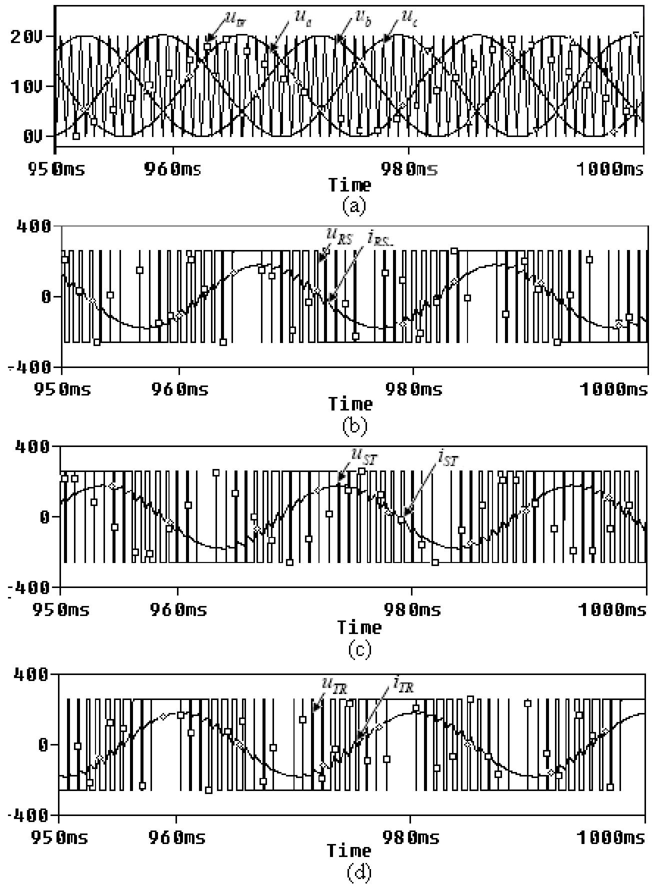

Figure 8.a) Sinusoidal modulation signals of the FBI; b) c) d) The output waveforms of FBI

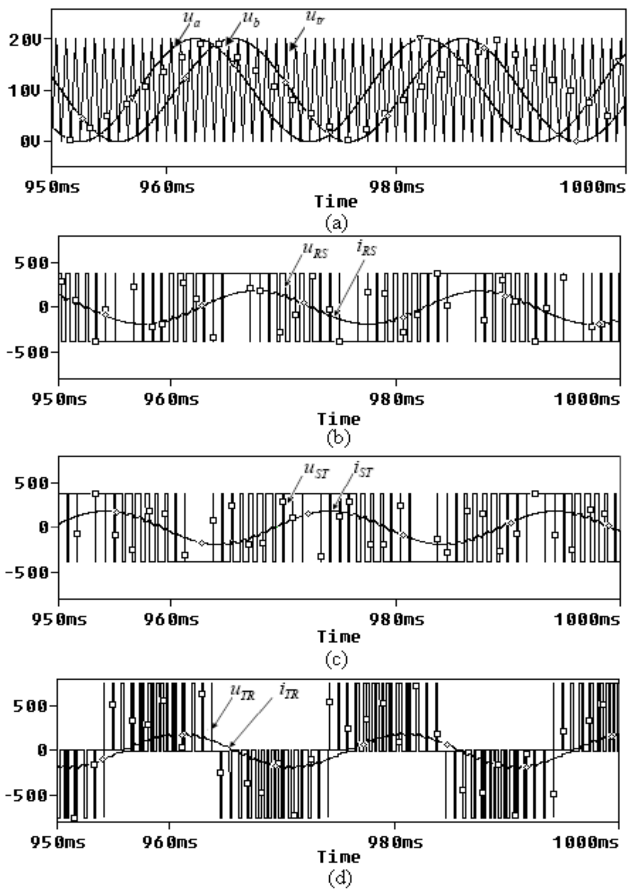

Figure 9.a) Sinusoidal modulation signals of the IBI; b) c) d) The output waveforms of the double-branch inverter

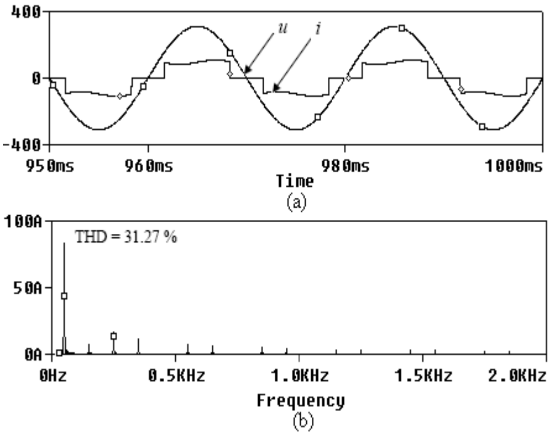

Figure 10.a)Input phase converter voltage and current from Figure 1; b) Input phase current harmonic distribution from Figure 1

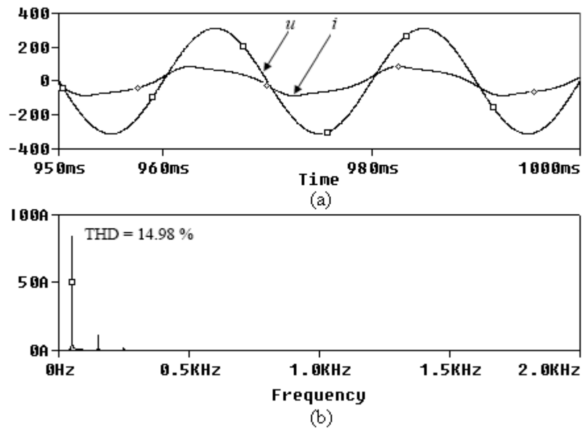

Figure 11.a) Input phase converter voltage and current from Figure 3; b) Input phase current harmonic distribution from Figure 3

IV. SIMULATION RESULTS

According to the procedure presented in Section III, a RNSIC converter with a three phase IBI was designed and simulated. The 'n' – ratio was set to a value equal to 1.6, the inductances $L_1 - L_3$ and the capacitors $C_1 - C_3$ (Figure 3a) are determined with (4), (15) and (16) and are equal to 10mH and 140μF, respectively.

The comparison is done against a FBI with a three phase bridge diode rectifier (Figure 1) driven through a sinusoidal PWM modulation. In Figures 8a and 9a, the control signals, the output inverter voltage and current are plotted. Both converters use a sinusoidal modulation with a modulation factor equal to one.

In Figure 9, the voltage u_{TR} is unipolar, whereas both voltages u_{RS} and u_{ST} are bipolar. All three voltages have the same fundamental amplitude.

The simulation results under the same load conditions associated to the circuits presented in Figure 1 and Figure 3 are depicted in Figures 10 and 11. In Figure 11a, the network phase current has almost the same phase with the network phase voltage, because the converter works at maximum nominal output power. The harmonics distribution of the network phase current is presented in Figures 10b and 11b.

From the simulations it can be concluded that the circuit proposed in Figure 3 ensures a THD (total harmonic distortion) of 14.98 %, significantly better than the standard circuit depicted in Figure 1, which has a THD value of 31.27%.

V. CONCLUSION

This paper presents a new static frequency converter with RNSIC converter and double branch inverter for supplying three – phase asynchronous motors. Its performances are assessed in comparison to the standard converter. From both the simulation results and the theoretical evaluation, several aspects can be concluded. Firstly, the injected harmonics into the system are reduced two times. Secondly, the circuit has the ability to protect the load from overcurrent shocks. Thirdly, the total cost of implementing the circuit may be less than the cost implied by the standard converter. Finally, the circuit output power can be controlled through the modulation factor.

The proposed circuit can be used in a wide variety of applications in which the mechanical torque of the motor is proportional to the spin velocity of the motor (for instance water evacuation pumps). In this case, the output frequency of the converter can be controlled as a function of the phase difference between the voltage of the network and the absorbed current. If the input of the RNSIC has a capacitive behavior (Figure 5) then the frequency can be increased, whereas if the input of the RNSIC has an inductive behavior, the frequency has to be decreased. The ratio v/f can be maintained constant through the proper adjustment of the modulation factor, according to both the frequency and the real – time DC link value (V_D).

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